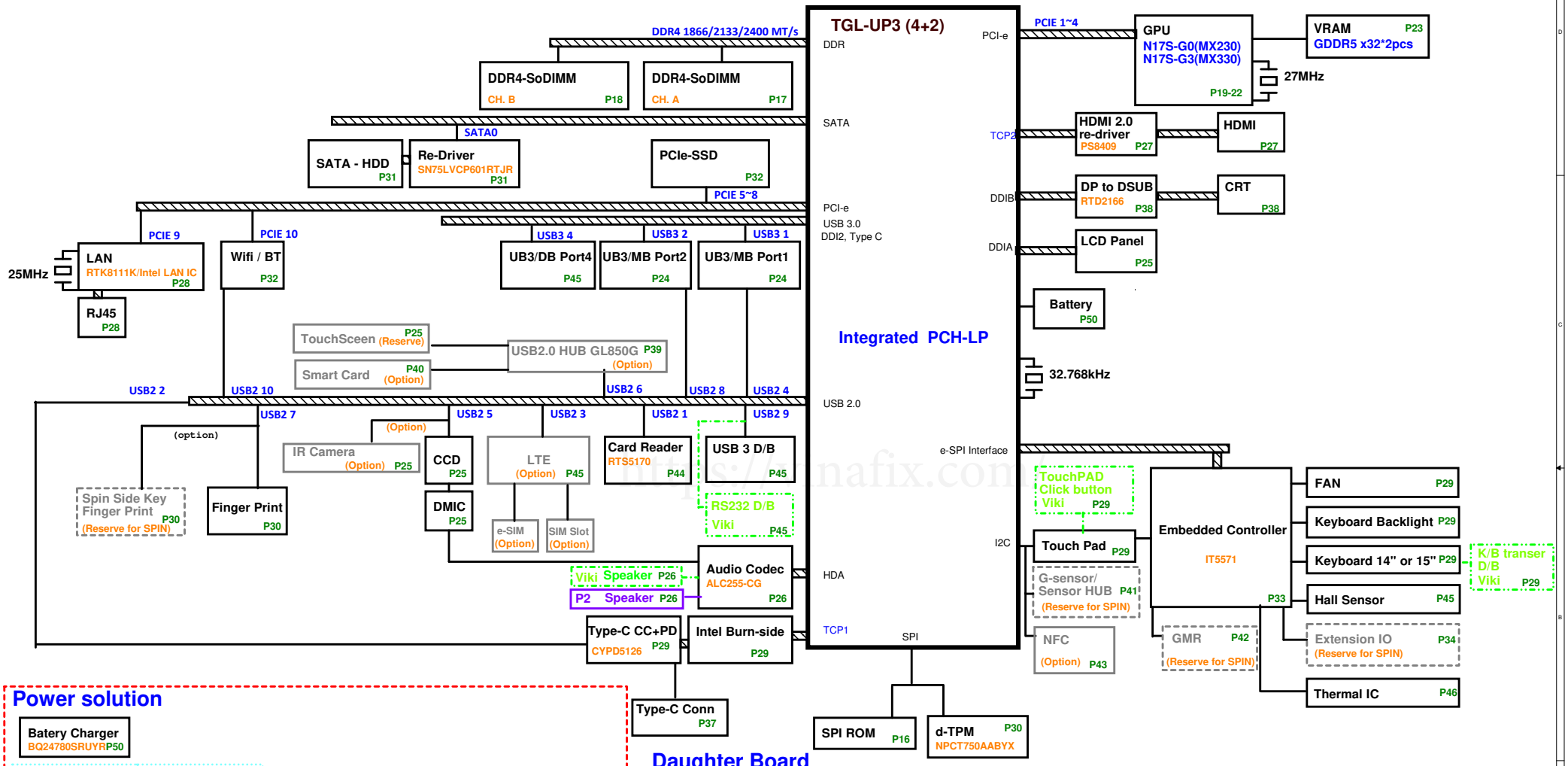
Z8IA(Timapni_TL)/ZAIA (BassDrum_TL) TigerLake-UP3 Block Diagram (DIS/UMA)

01



Power solution

- Batery Charger BQ24780SRUYR P50
- +3VPCU RT6256BGQUF P51
- +5VPCU RT6258CGQUF P51
- +VCCIN RT3612EBGQW P53
- +VGPU_CORE P56 RT8813DGQW
- +3V/+3V_S5 AOZ1331ADI P51
- +5V/+5V_S5 AOZ1331ADI P51
- +VCCIN_AUX RT6543AGQW P54
- +1.35V_GFX G5335QT2U P57
- +1.03_GFX G9336ADJTP1U P58
- +1.2VSUS/+VDDQ_VTT/+VDDQ RT8231BGQW P52
- +1.8V_S5 JW5213DFND_TRPBF P55
- +1.2V AOSS32334C P52
- +1.8V AOSS32334C P55
- +1V8_AON/+1V8_GFX_MAIN JW7110DFNC P58
- +2.5V_SUS G5719CTB1U P52
- +1.5V JW5222RSOTB_TRPBF P55
- +VCCSTG/+VCCST EMF11N02J P47

Daughter Board

- GMR sensor/B (Reserve for SPIN) P42
- Spin side key/B (Reserve for SPIN) P30
- LTE/B P45
- USB3/B P45
- RS232 D/B Viki P45
- K/B transer D/B Viki P29
- TouchPAD Click button Viki P29

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : IN4
LAYER 9 : SGND
LAYER 10 : BOT

SKU remind

1)LTE SKU notice
a.LTE SKU without HDD (14" & 15")
b.LTE SKU without IR CCD (14" & 15)
c.LTE SKU without Touch Panel (14")

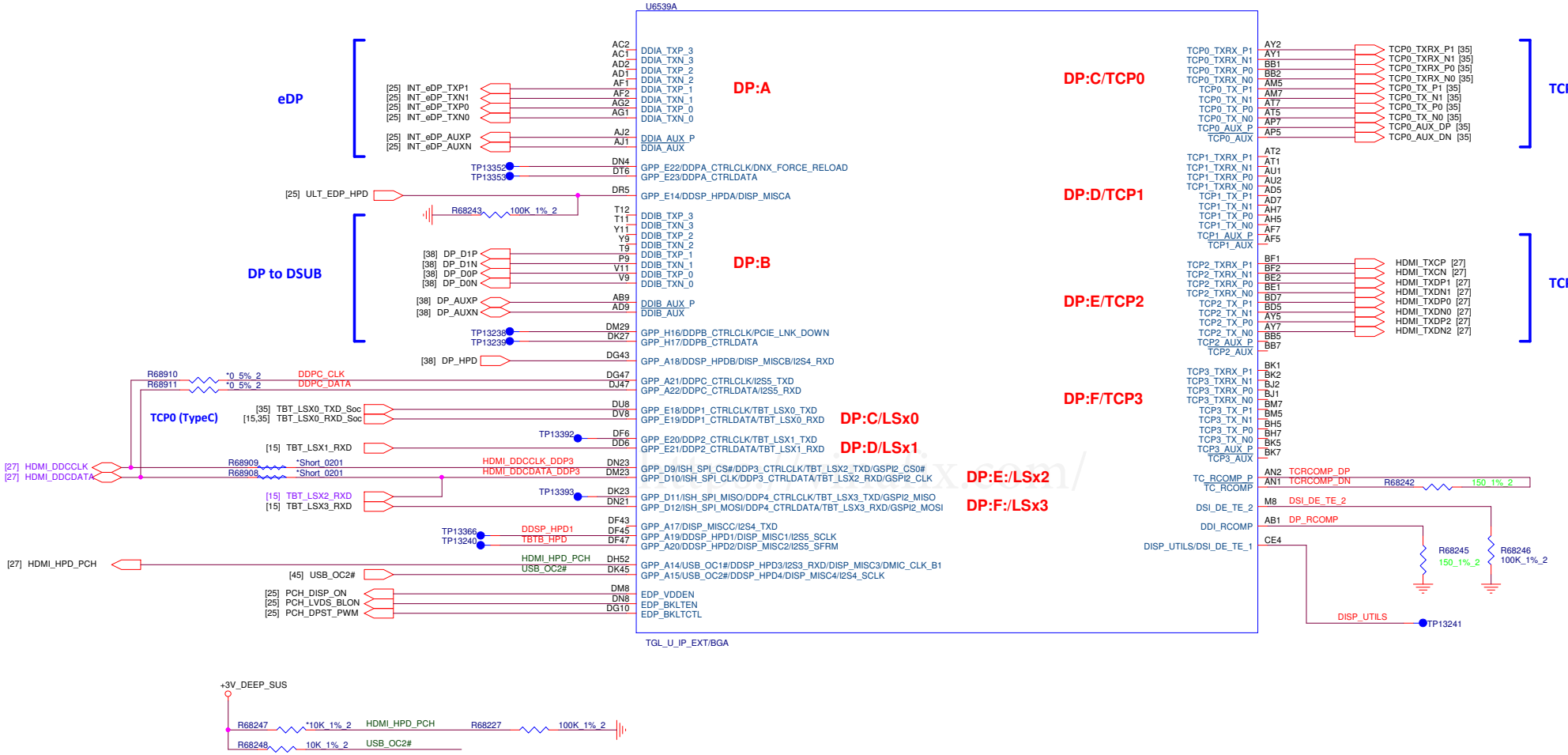
2)HDD/SSD/TSN didn't BOM Option. Others OPTION/D.R by tender requirement?

3)M.S or S3. MB ID decision system support no follow to Storage Config.
a.SSD + HDD
b.SSD only
c.HDD only

Quanta Computer Inc.
PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	Intel Block Diagram	1A

Date: Tuesday, October 06, 2020 Sheet 1 of 62



Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number	Rev
	TGL-U 1/14 (DDI/TBT/eDP)	1A
Date: Tuesday, October 06, 2020	Sheet 2 of 62	

TIGER LAKE Processor DDR4/4X

03

DDR CHANNEL A

DDR CHANNEL B

U6539B

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

DDR4/LP4/LP5/LP5 CMD Flip

TGL_U_IP_EXT/BGA

U6539C

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

TGL_U_IP_EXT/BGA

U6539D

TGL_U_IP_EXT/BGA

+1.2VSUS

+3V_S5

+3V

DRAM_RESET#

DDR_VTTT_PG_CTRL [52]

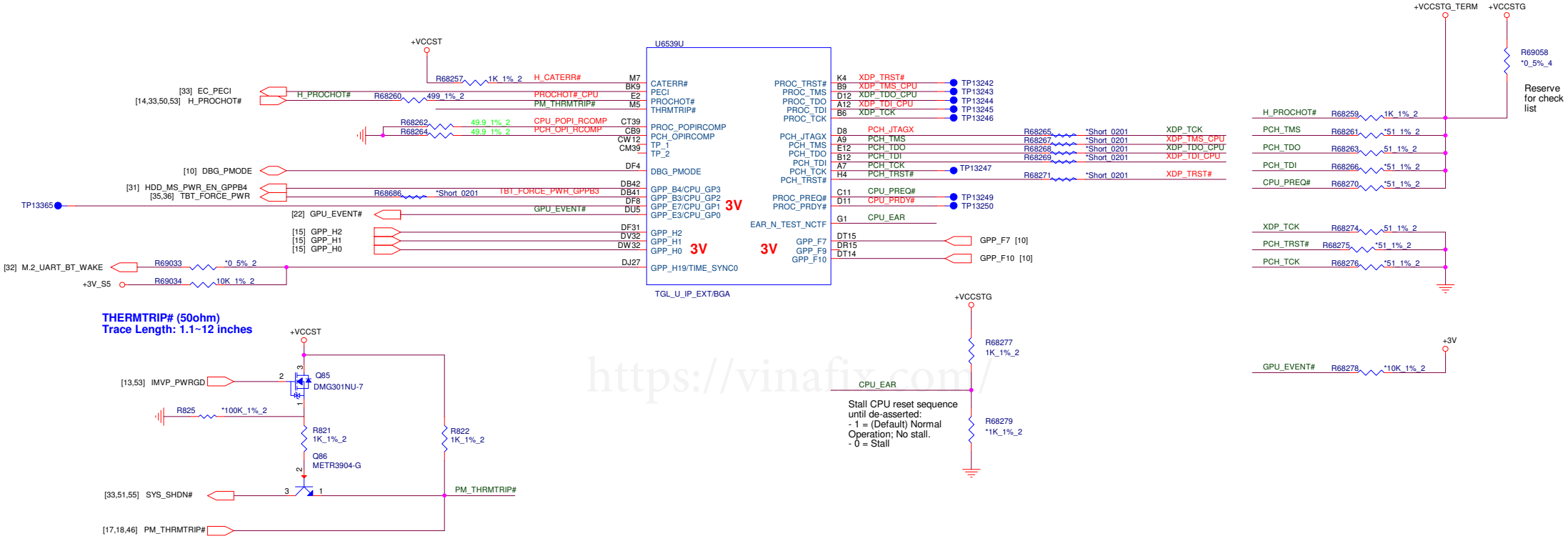
DDR_VTT_CTRL

SMDDR_VREF_DQ1_M3 [18]

Quanta Computer Inc.

PROJECT : Z8IA_ZAIA

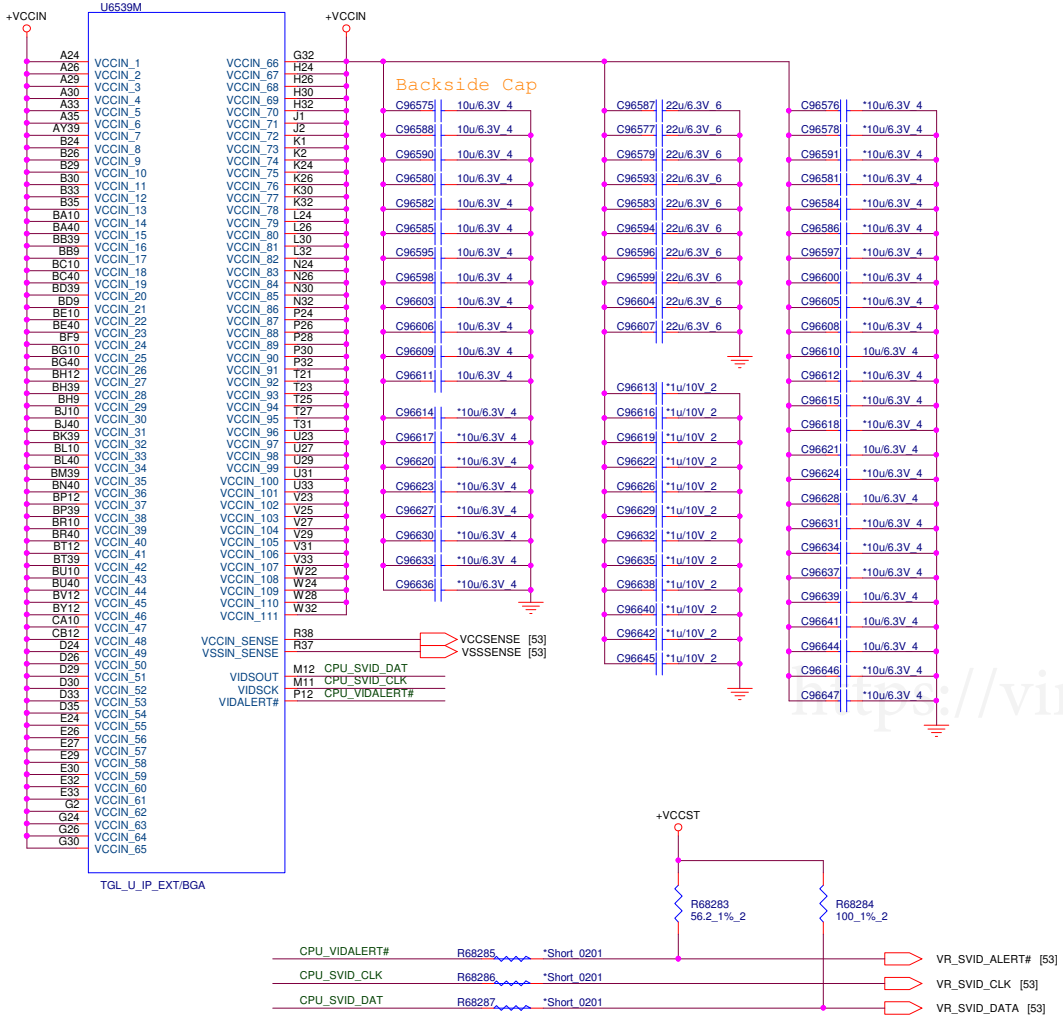
Size	Document Number	Rev
	TGL-U 2/14 (LPDDR4 I/F)	1A
Date: Tuesday, October 06, 2020	Sheet 3 of 62	



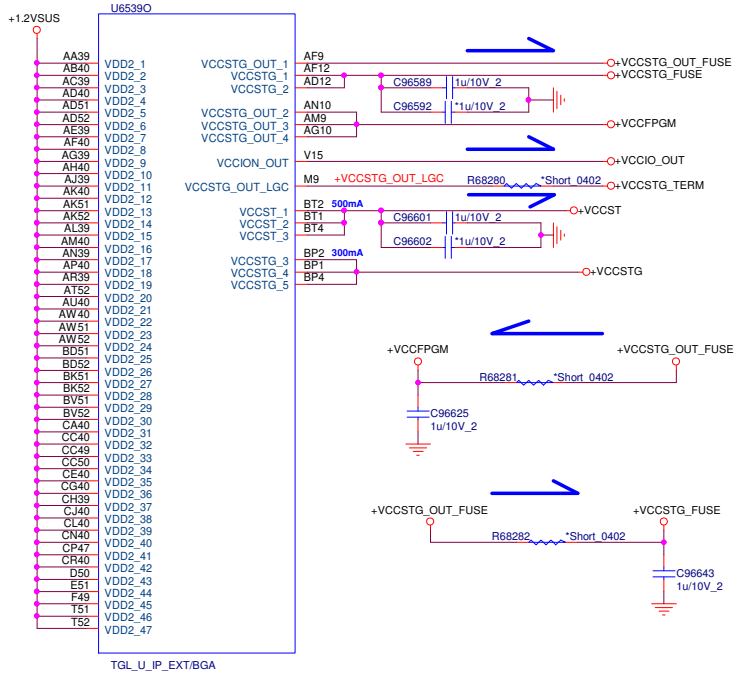
https://vinafix.com/

Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number: TGL-U 3/14 (CPU MISC/JTA)	Rev: 1A
Date: Tuesday, October 06, 2020	Sheet 4 of 62	

+VCCIN: 65A

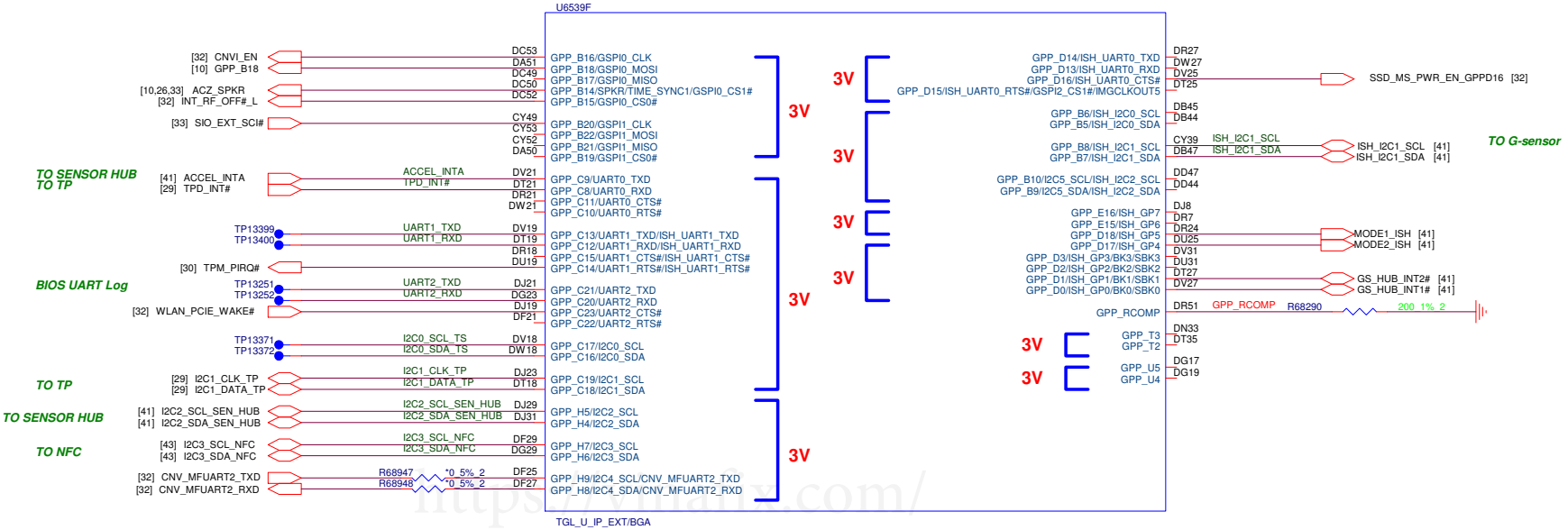


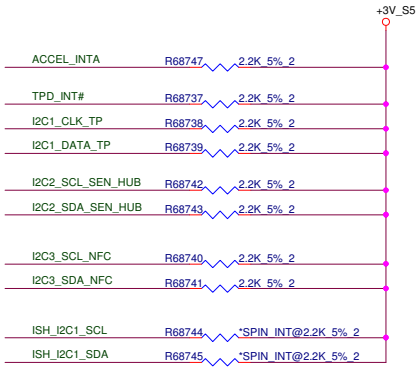
+1.2VSUS: 1.5A



https://vinafix.com/
Vinafix.com

Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number: TGL-U 4/14 (VCCIN/VDDQ)	Rev: 1A
Date: Tuesday, October 06, 2020	Sheet 5 of 62	





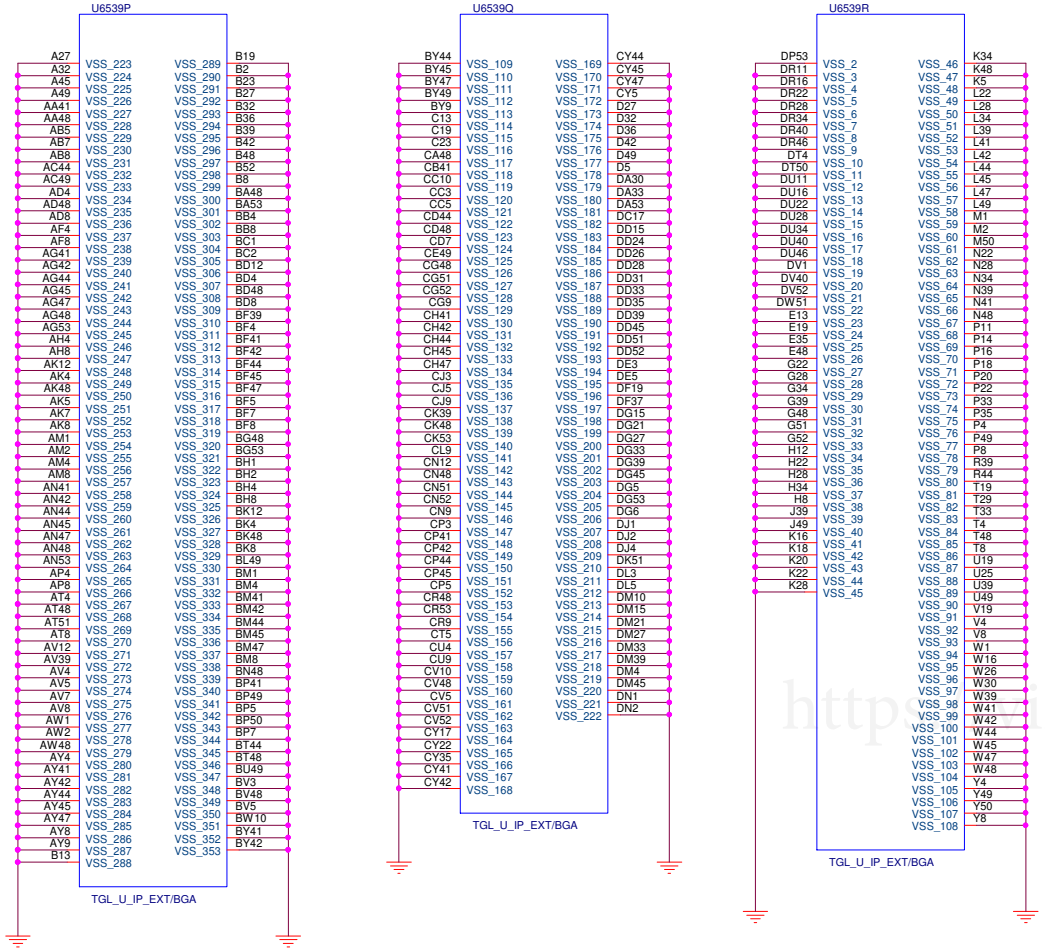
https://vnafix.com/

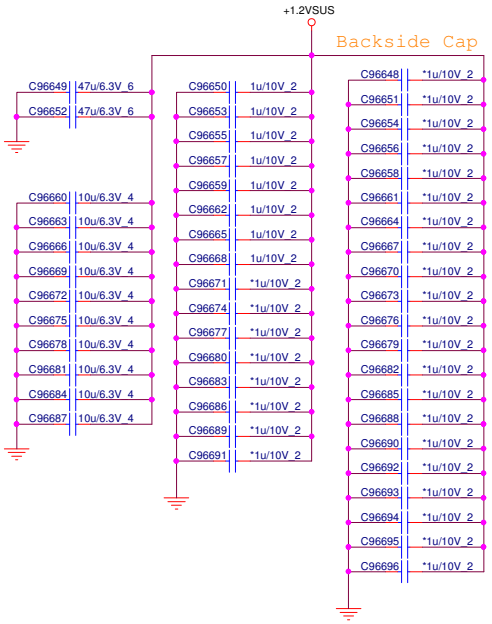
Quanta Computer Inc.

PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	TGL-U 5/14 (I2C/ISH)	1A

Date: Tuesday, October 06, 2020 Sheet 6 of 62





https://vinafix.com/

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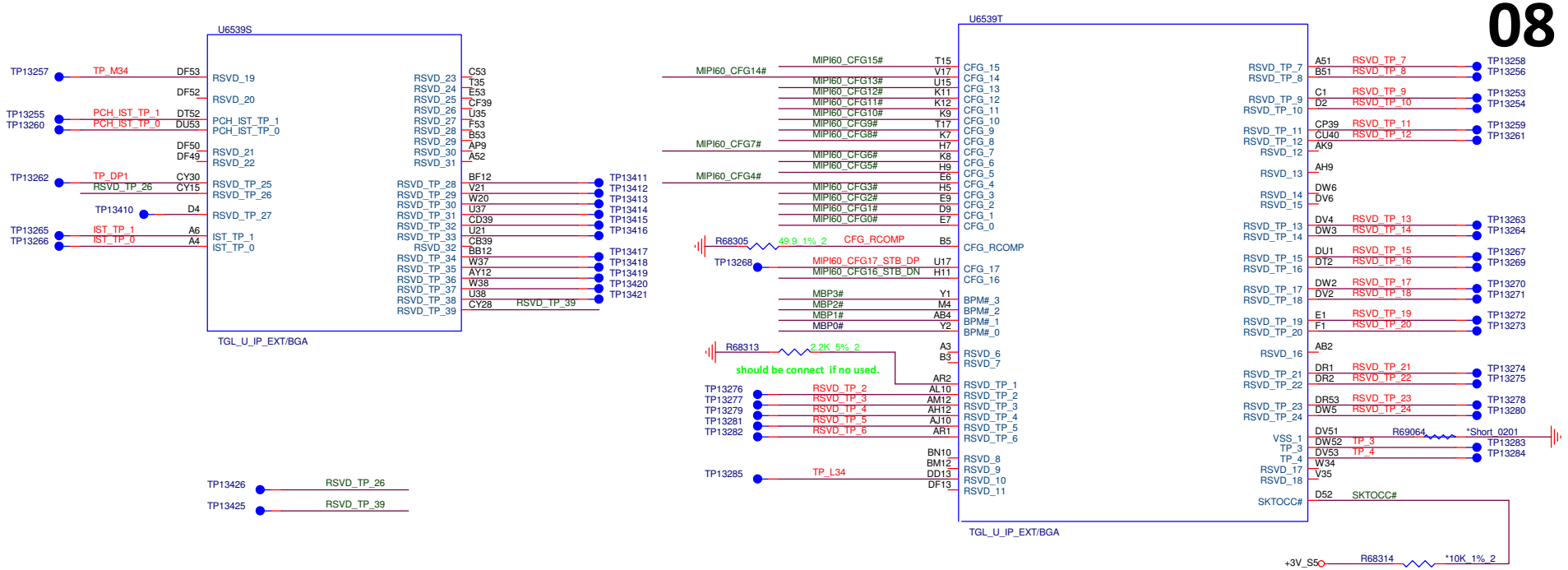
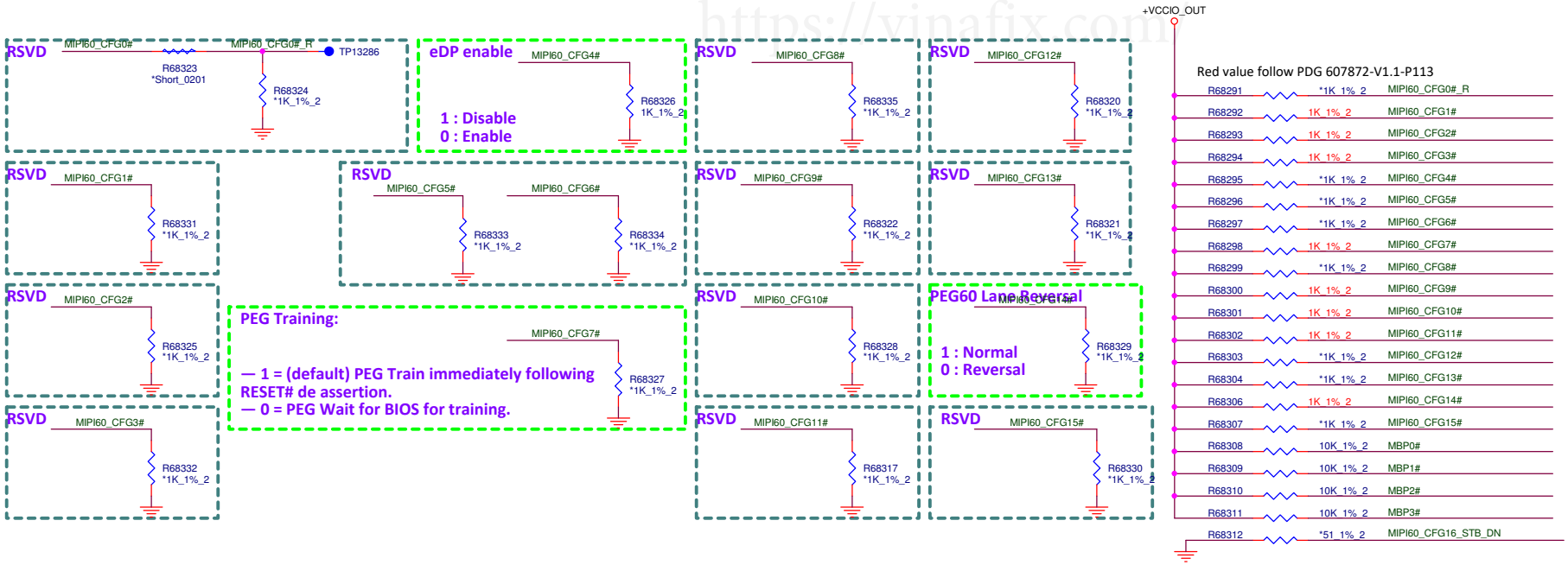
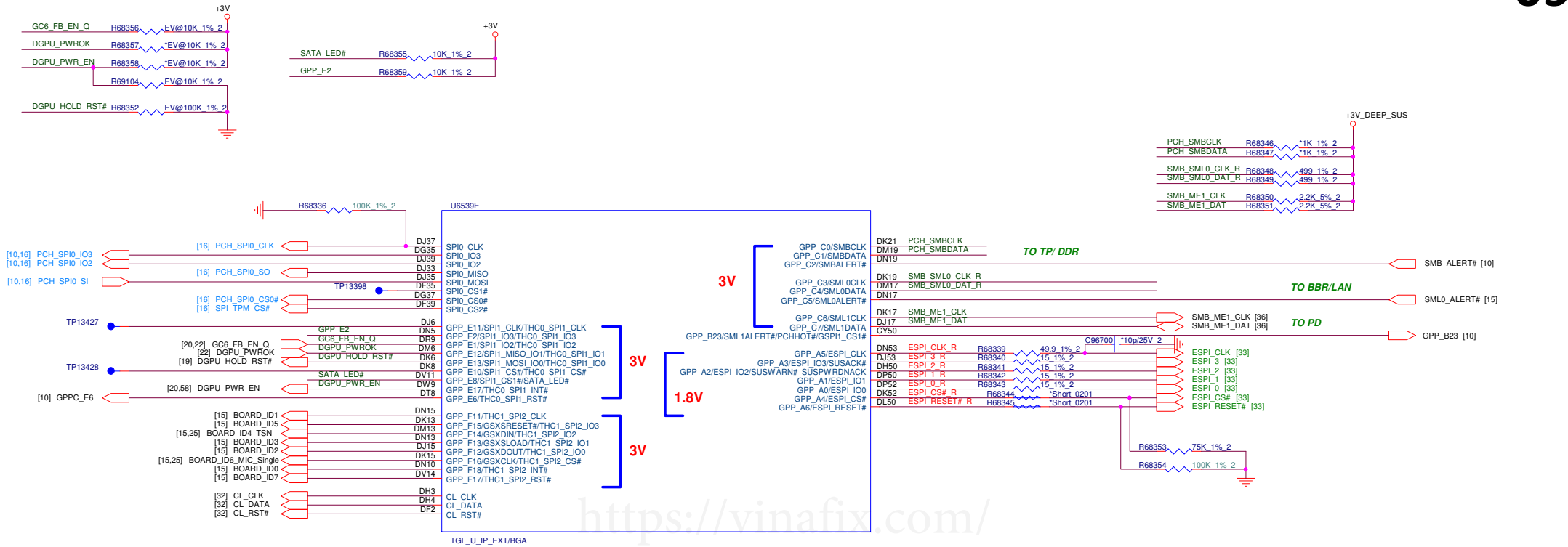
Quanta Computer Inc.			
PROJECT : Z8IA_ZAIA			
Size	Document Number		Rev
	TGL-U 6/14 (GND)		1A
Date: Tuesday, October 06, 2020	Sheet 7 of 62		



https://vinafix.com



Quanta Computer Inc.			
PROJECT : Z8IA_ZAIA			
Size	Document Number		Rev
	TGL-U 7/14 (RSVD/XDP)		1A
Date: Tuesday, October 06, 2020		Sheet 8 of 62	

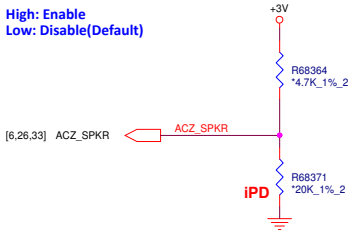


Quanta Computer Inc.

PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	TGL-U 8/14 (SMBus/SPI)	1A
Date: Tuesday, October 06, 2020	Sheet 9 of 62	

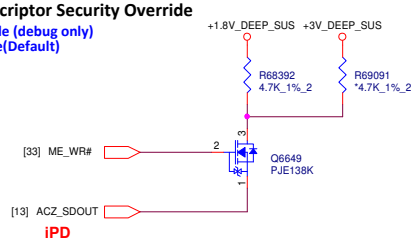
TOP SWAP OVERRIDE
High: Enable
Low: Disable(Default)



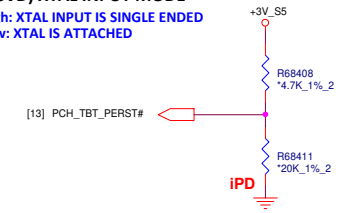
Port Voltage-GPP_D10

Page15

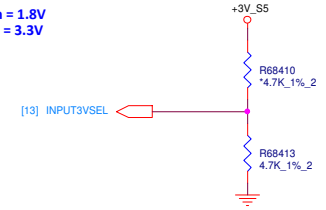
Flash Descriptor Security Override
High: Disable (debug only)
Low: Enable(Default)



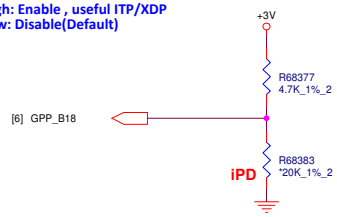
(RSVD) XTAL INPUT MODE
High: XTAL INPUT IS SINGLE ENDED
Low: XTAL IS ATTACHED



SPIVCCIOSEL
High = 1.8V
Low = 3.3V



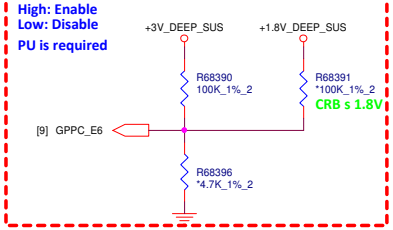
NO REBOOT
High: Enable , useful ITP/XDP
Low: Disable(Default)



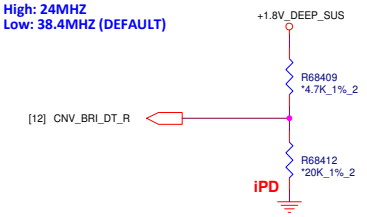
Port Voltage-GPP_D12

Page15

(RSVD) JTAG ODT DISABLE
High: Enable
Low: Disable
PU is required

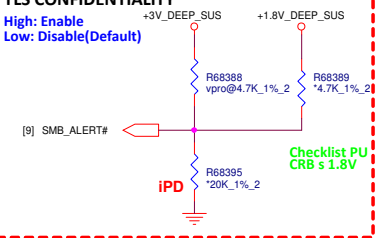


XTAL FREQUENCE SEL
High: 24MHZ
Low: 38.4MHZ (DEFAULT)

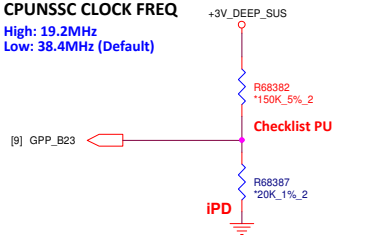


MAF/SAF STRAP
High: SAF ENABLE
Low: MAF ENABLE
WEAK INTERNAL PD 20K

TLS CONFIDENTIALITY
High: Enable
Low: Disable(Default)



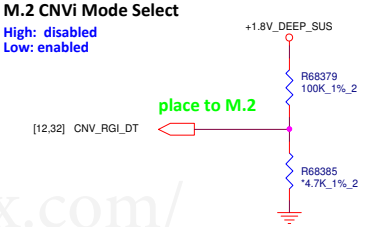
CPUNSSC CLOCK FREQ
High: 19.2MHz
Low: 38.4MHz (Default)



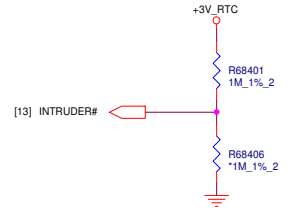
Port Voltage-GPP_E19

Page15

M.2 CNVi Mode Select
High: disabled
Low: enabled



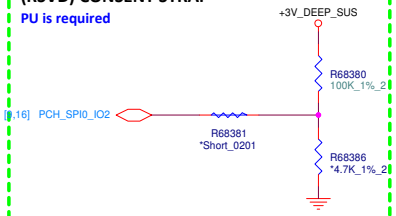
FOR FAST BOOT
High : 140MSEC WITH 3.3V FLASH SUPPORT



Boot Strap 0

Page15

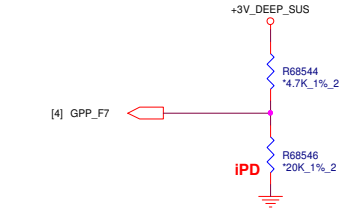
(RSVD) CONSENT STRAP
PU is required



Port Voltage-GPP_E21

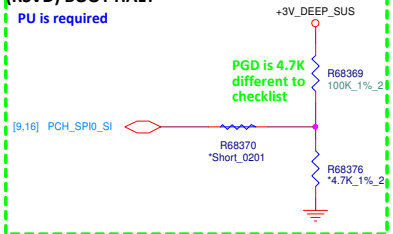
Page15

Reserved

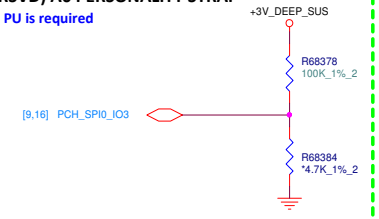


THC0_SPI1_CLK
THC0_SPI1 Clock: THC SPI1 clock output from PCH. Supports 20 MHz, 33 MHz and 50 MHz.

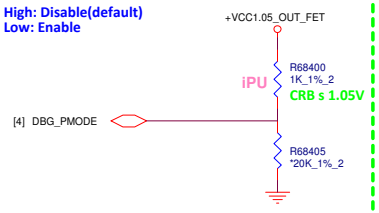
(RSVD) BOOT HALT
PU is required



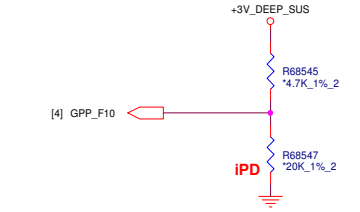
(RSVD) A0 PERSONALITY STRAP
PU is required



(RSVD) ITP PMODE
High: Disable(default)
Low: Enable



Reserved

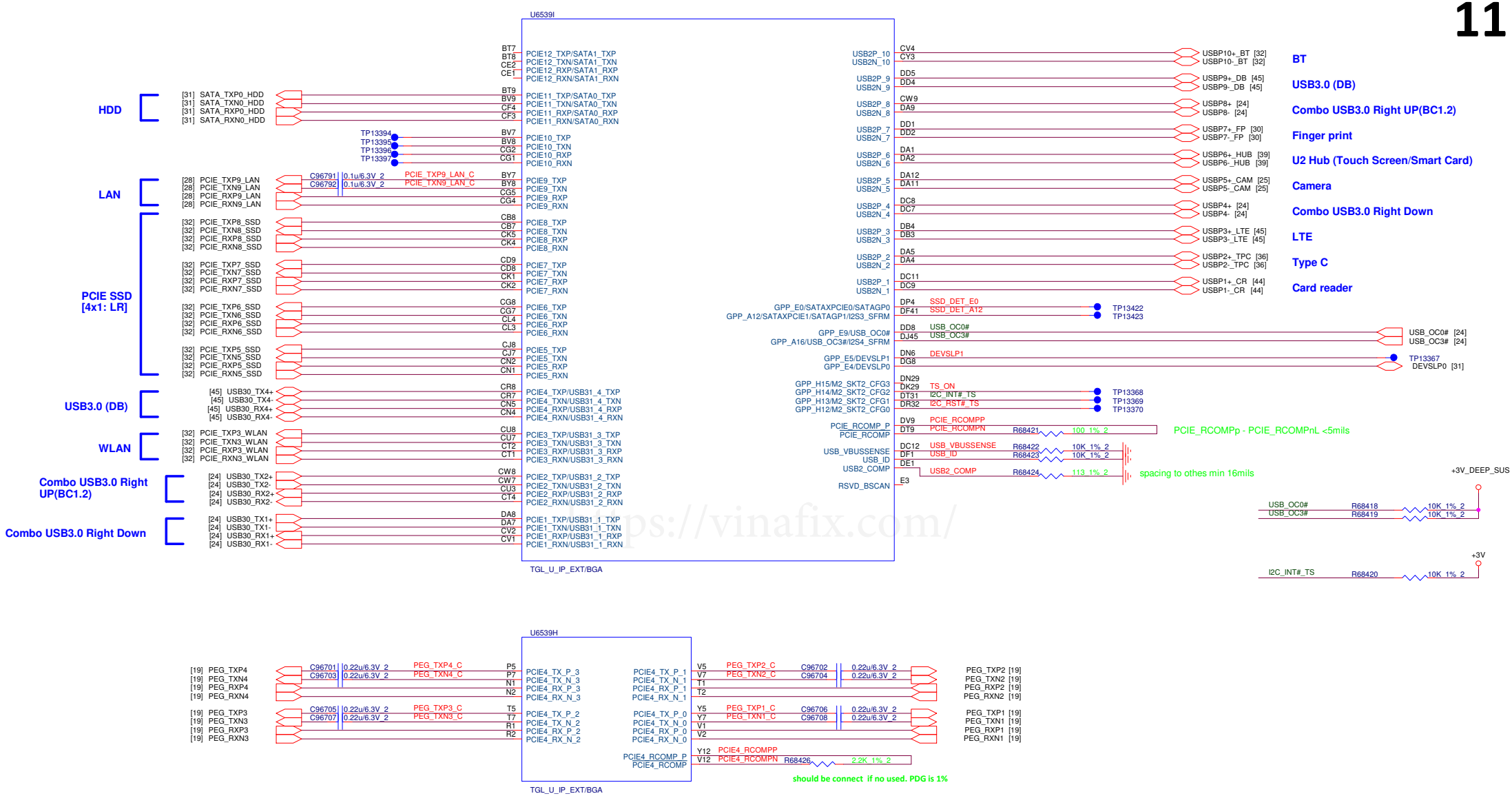


THC0_SPI1_CS#
THC0_SPI1 Chip Select: Used to select the touch devices if it is connected to THC0_SPI1 interface.

https://vinafix.com/

Quanta Computer Inc.
PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	TGL-U 9/14 (HW STRAP)	1A
Date: Tuesday, October 06, 2020	Sheet 10 of 62	



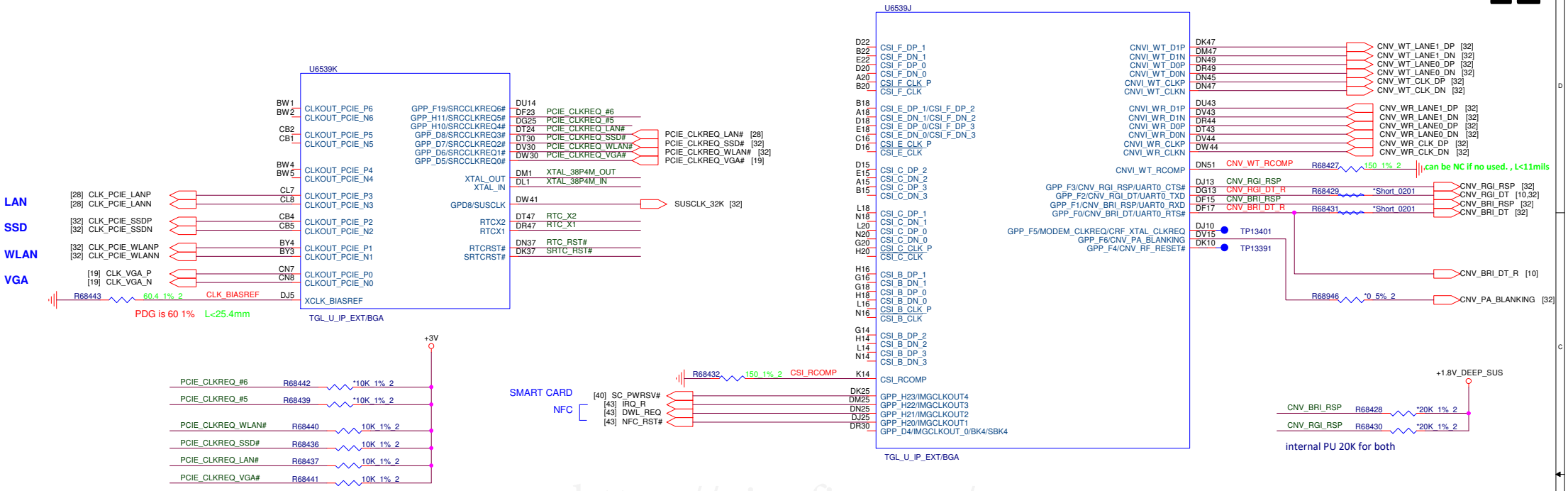
https://vinafix.com/

Quanta Computer Inc.

PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	TGL-U 10/14(USB/PCIE/SAT)	1A

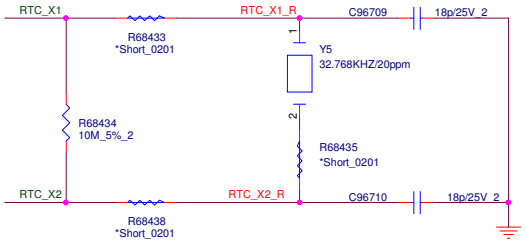
Date: Tuesday, October 06, 2020 Sheet 11 of 62



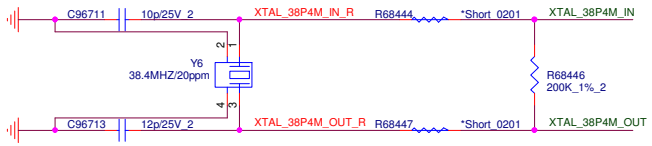
https://vinafix.com/

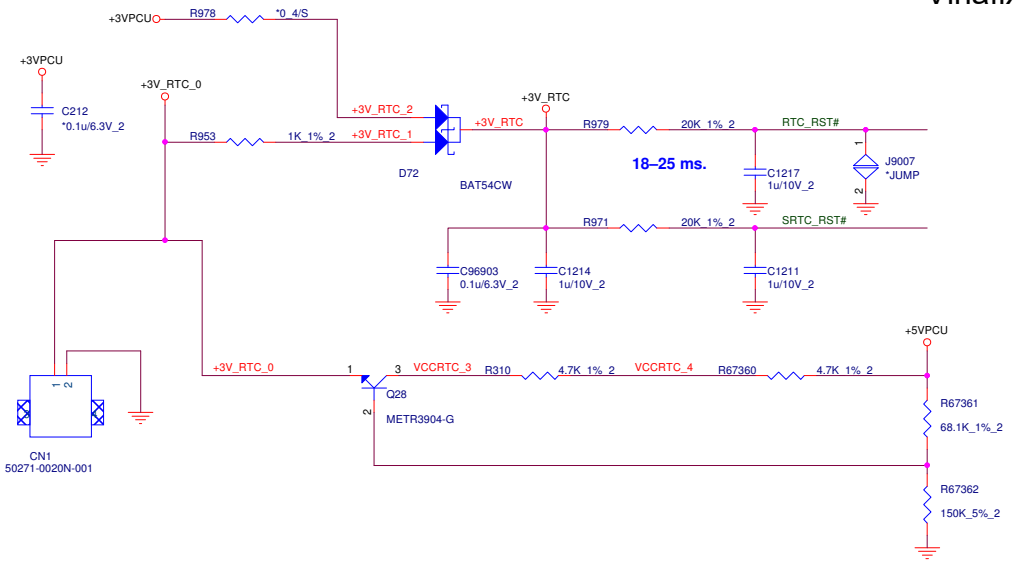
RTC Circuitry(RTC)

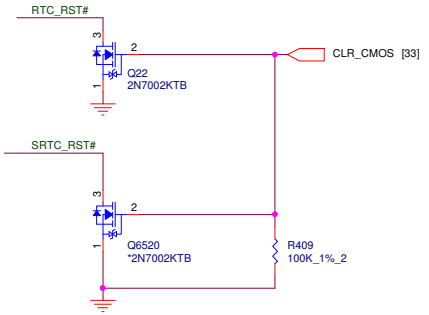
Vinafix.com



Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace



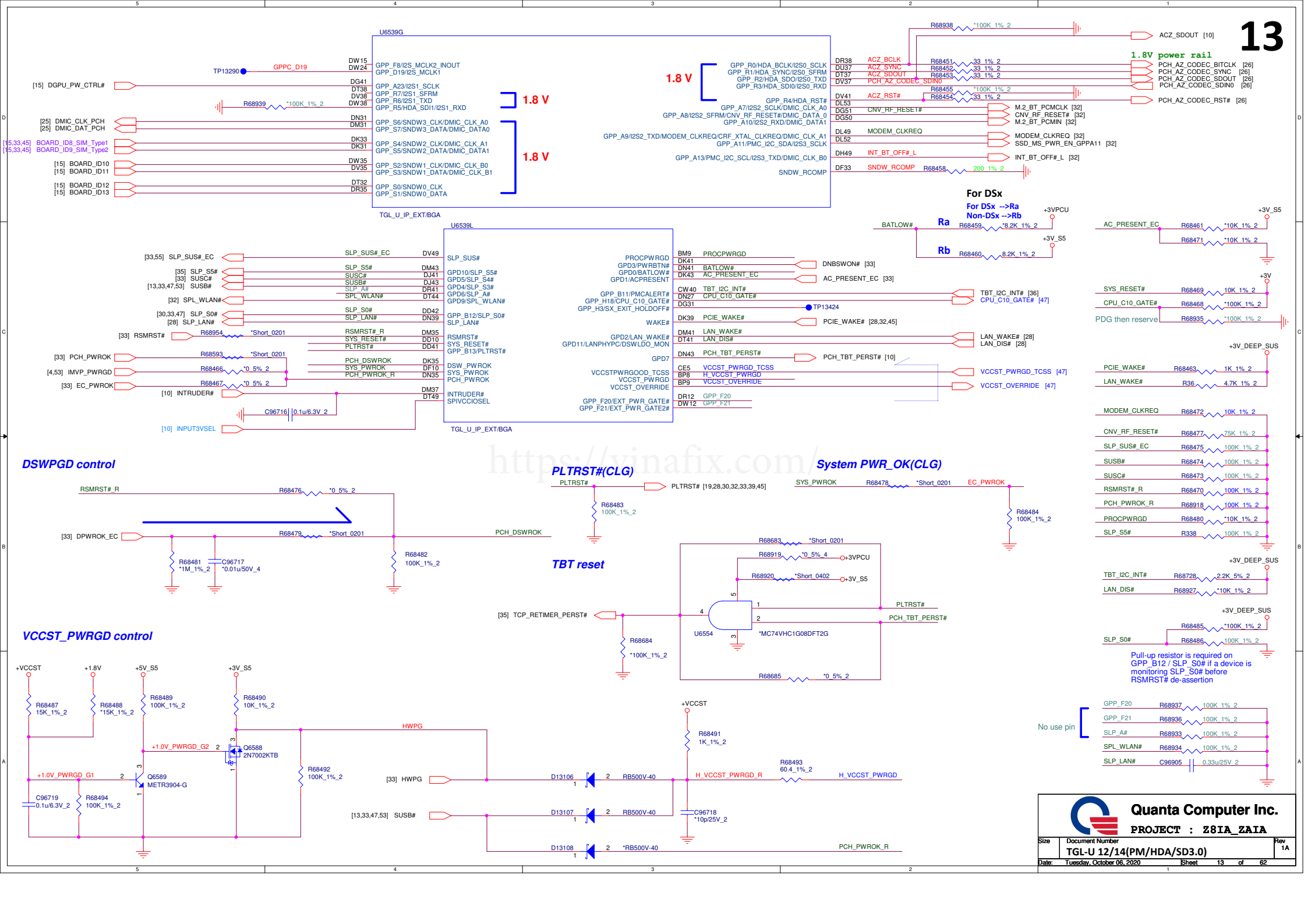




Quanta Computer Inc.
PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	TGL-U 11/14(CSI/CNVi/CLK)	1A

Date: Tuesday, October 06, 2020 Sheet 12 of 62



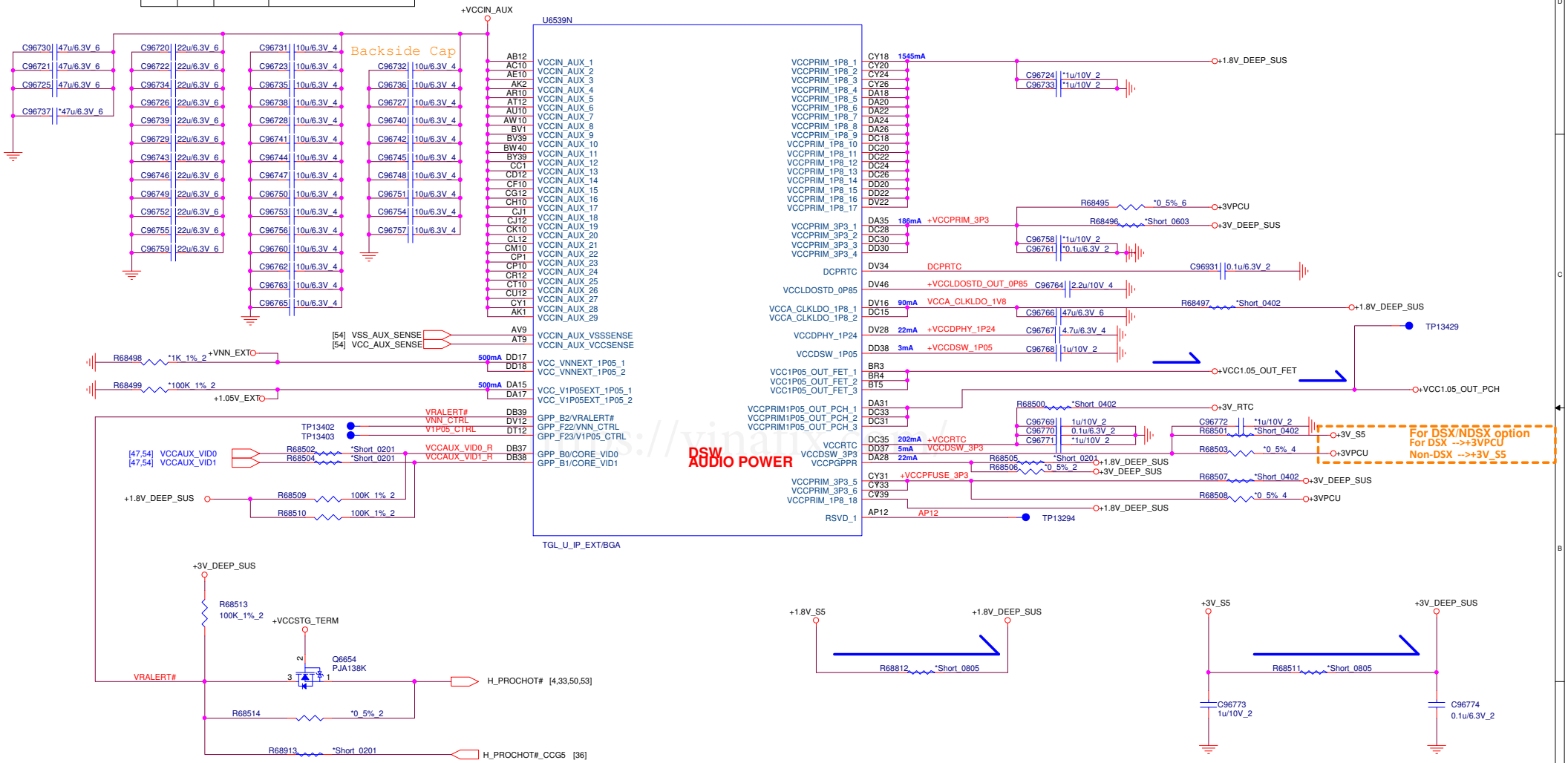
https://vinafix.com/

Quanta Computer Inc.
PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	TGL-U 12/14(PM/HDA/SD3.0)	1A
Date: Tuesday, October 06, 2020	Sheet 13 of 62	

VID1	VID0	Voltage	Usage
0	0	0	Power saving
0	1	1.1	Power saving
1	0	1.65	Full Current
1	1	1.8	Initial boot oe Full current

+VCCIN_AUX: 27A



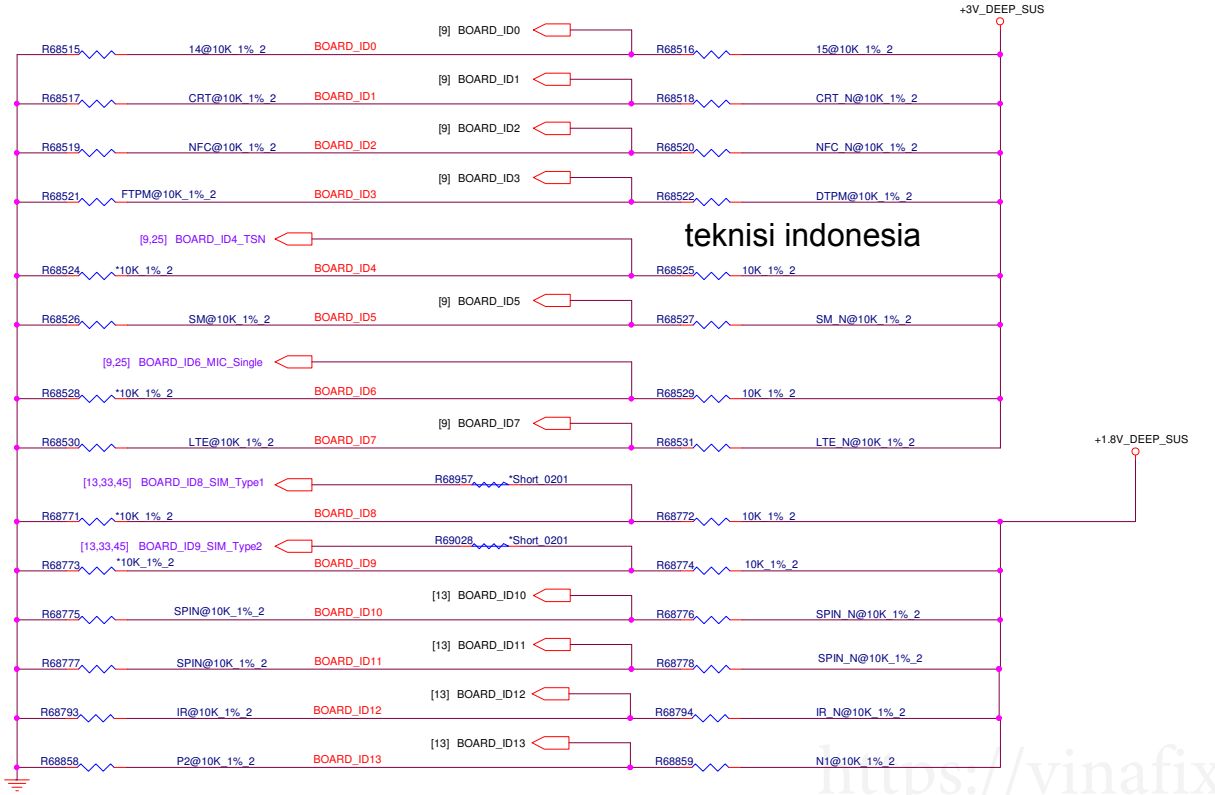
https://vinafix.com/

Quanta Computer Inc.

PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	TGL-U 13/14(PCH POWER)	1A

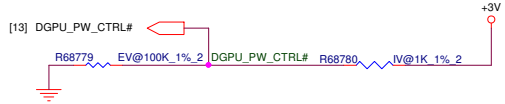
Date: Tuesday, October 06, 2020 Sheet 14 of 62



teknisi indonesia

	Low	High
BOARD_ID0	14@	15@
BOARD_ID1	CRT@	CRT_N@
BOARD_ID2	NFC@	NFC_N@
BOARD_ID3	FTPM@	DTPM@
BOARD_ID4	TSN@ (Cable control)	TSN_N@ (Default)
BOARD_ID5	SM@	SM_N@
BOARD_ID6	MIC_Single@ (Cable control)	MIC_Dual@ (default)
BOARD_ID7	LTE@	LTE_N@
BOARD_ID8	SIM Card type	11 : no support LTE 10 : u-SIM 01 : e-SIM 00 : u-SIM+e-SIM
BOARD_ID9		
BOARD_ID10	SEN_HUB@	SEN_HUB_N@
BOARD_ID11	SPIN@	SPIN_N@
BOARD_ID12	IR@	IR_N@
BOARD_ID13	P2@	N1@

DGPU_PW_CTRL#		
	high	UMA Only
	low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)



	DGPU_PW_CTRL#	VGA H/W Signal	Setup Menu	
UMA Only	1	UMA	Hidden	UMA boot
SG/Optimise	0	GPU	Hidden	GPU boot

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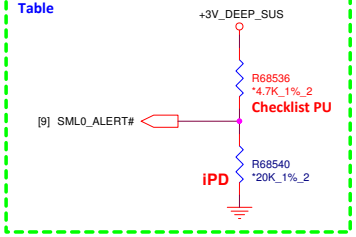
Boot Strap 0/1/2/3

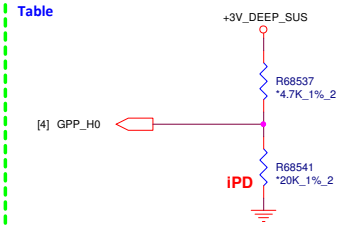
Boot Strap 0 GPP_C5

Table



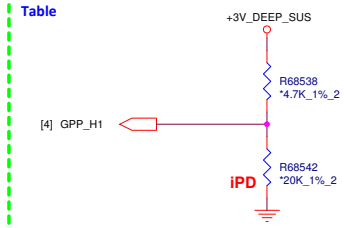
Boot Strap 1 GPP_H0

Table



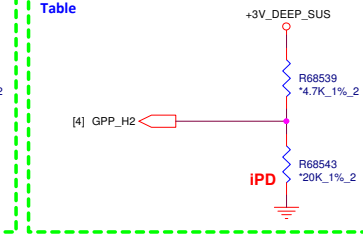
Boot Strap 2 GPP_H1

Table



Boot Strap 3 GPP_H2

Table

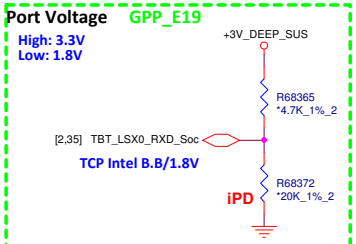


Boot Strap	4-bit boot strap configuration encodings
0000	BIOS/CSME on SPI & eSPI is enabled
0010	BIOS/CSME on SPI & eSPI is disabled
0100	BIOS on eSPI Peripheral Channel; CSME on master SPI
1000	BIOS/CSME on eSPI
1100	BIOS on eSPI peripheral Channel; CSME on slave SPI

TBT LSX PINS VCCIO CONFIGURATION

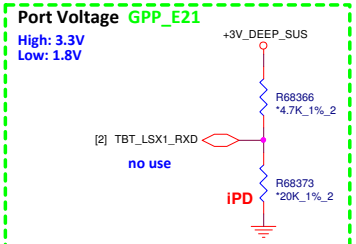
Port Voltage GPP_E19

High: 3.3V
Low: 1.8V



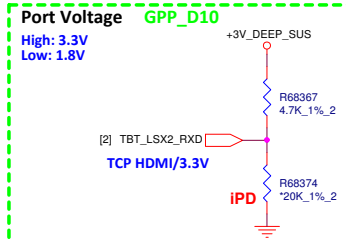
Port Voltage GPP_E21

High: 3.3V
Low: 1.8V



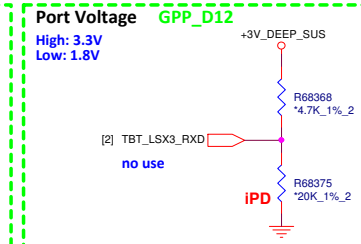
Port Voltage GPP_D10

High: 3.3V
Low: 1.8V



Port Voltage GPP_D12

High: 3.3V
Low: 1.8V



RING OSCILLATOR BYPASS

High: BYPASS MODE ENABLED
Low: RING OSCILLATOR
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

GPP_H3

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	TGL-U 14/14 (BLANK)	1A

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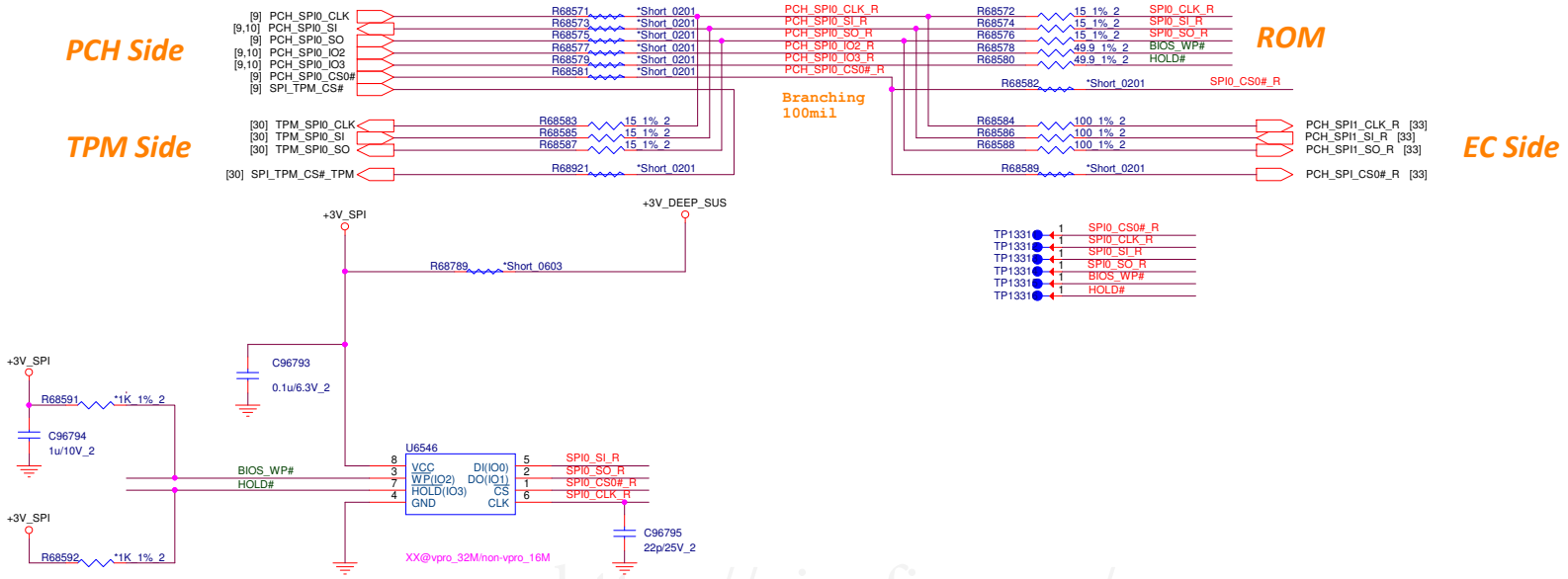
BIOS ROM 16M (CLG)



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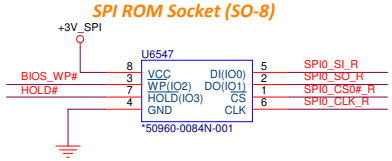
SPI ROM Socket (SO-8)

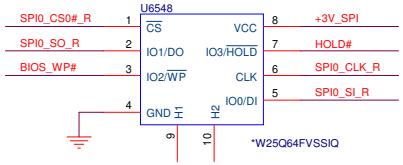


DG008000011

SPI ROM(SO-8)

Vender	Size	P/N
Socket		

SPI ROM Socket (WSON)



DFHS08FS046

SPI ROM(WSON)

Vender	Size	P/N
Socket		

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Size	Document Number	Rev
	Flash ROM (BIOS,EC)	1A

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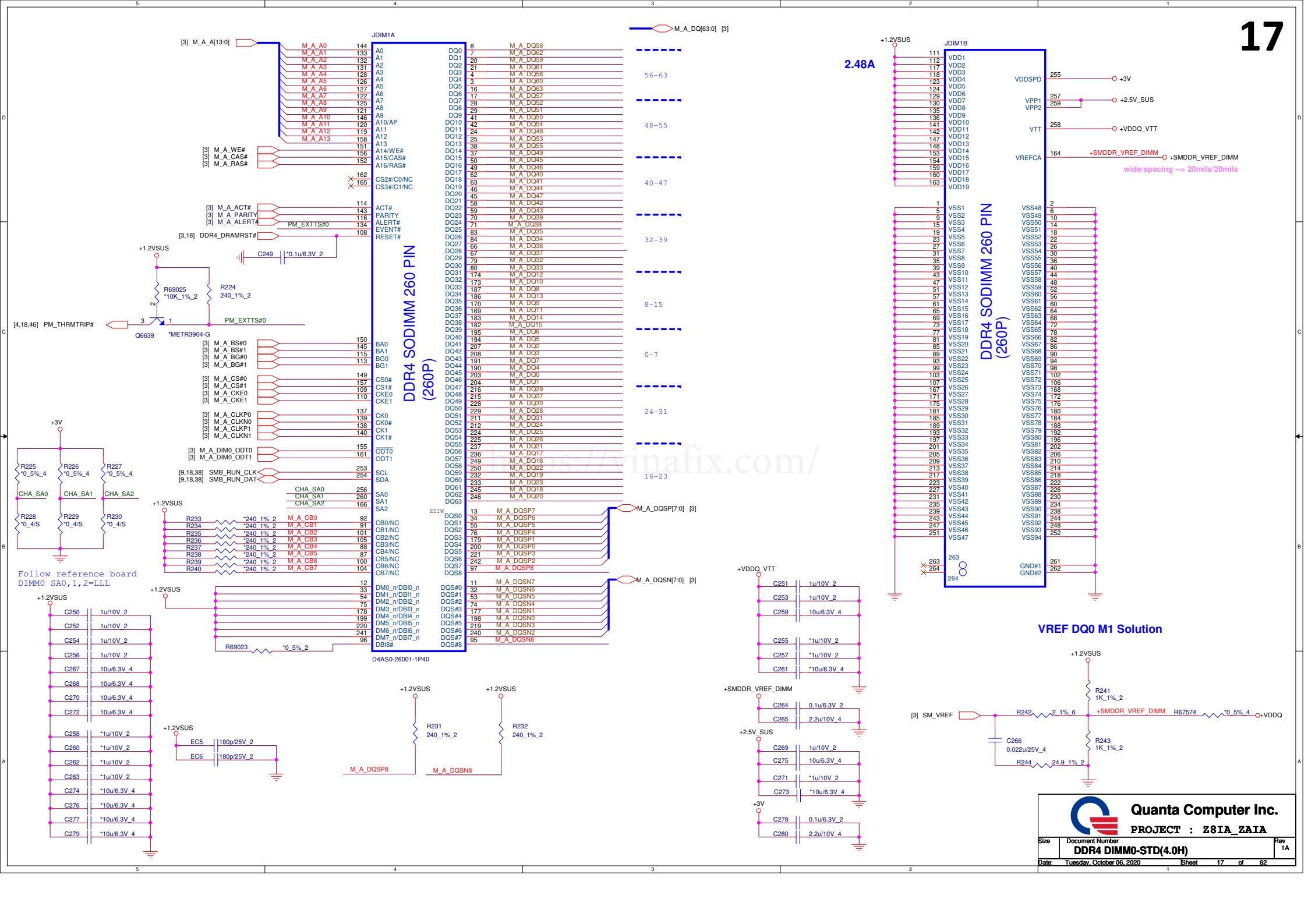
JDIM1A
DDR4 SODIMM 260 PIN
(260P)
D4AS0-26001-1P40
JDIM1B
DDR4 SODIMM 260 PIN
(260P)
2.48A
wide/spacing --> 20mils/20mils
VREF DQ0 M1 Solution
Follow reference board
DIMM0 SA0,1,2=LLL
56-63
48-55
40-47
32-39
8-15
0-7
24-31
16-23
Quanta Computer Inc.
PROJECT : Z8IA_ZAIA
DDR4 DIMM0-STD(4.0H)
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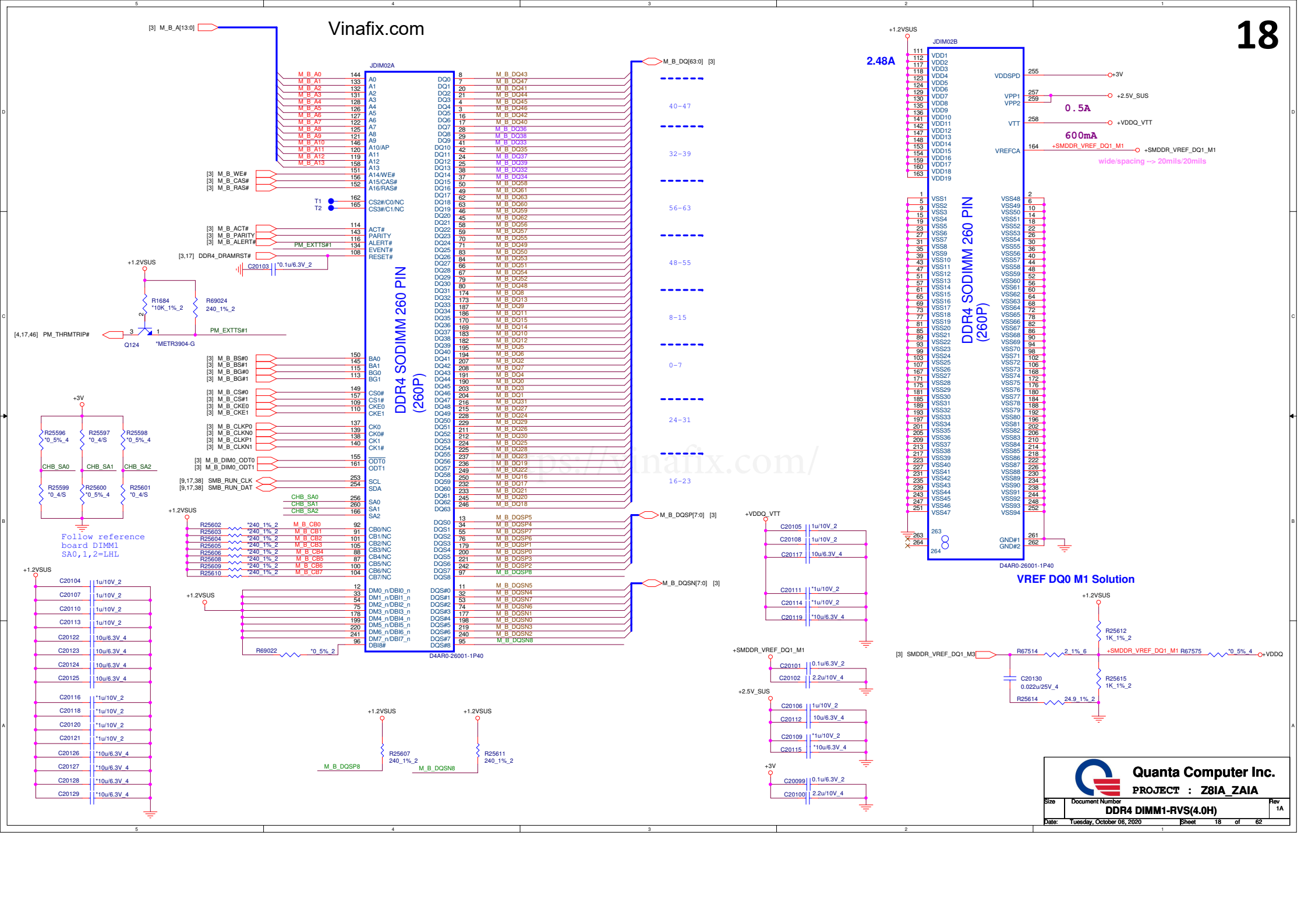
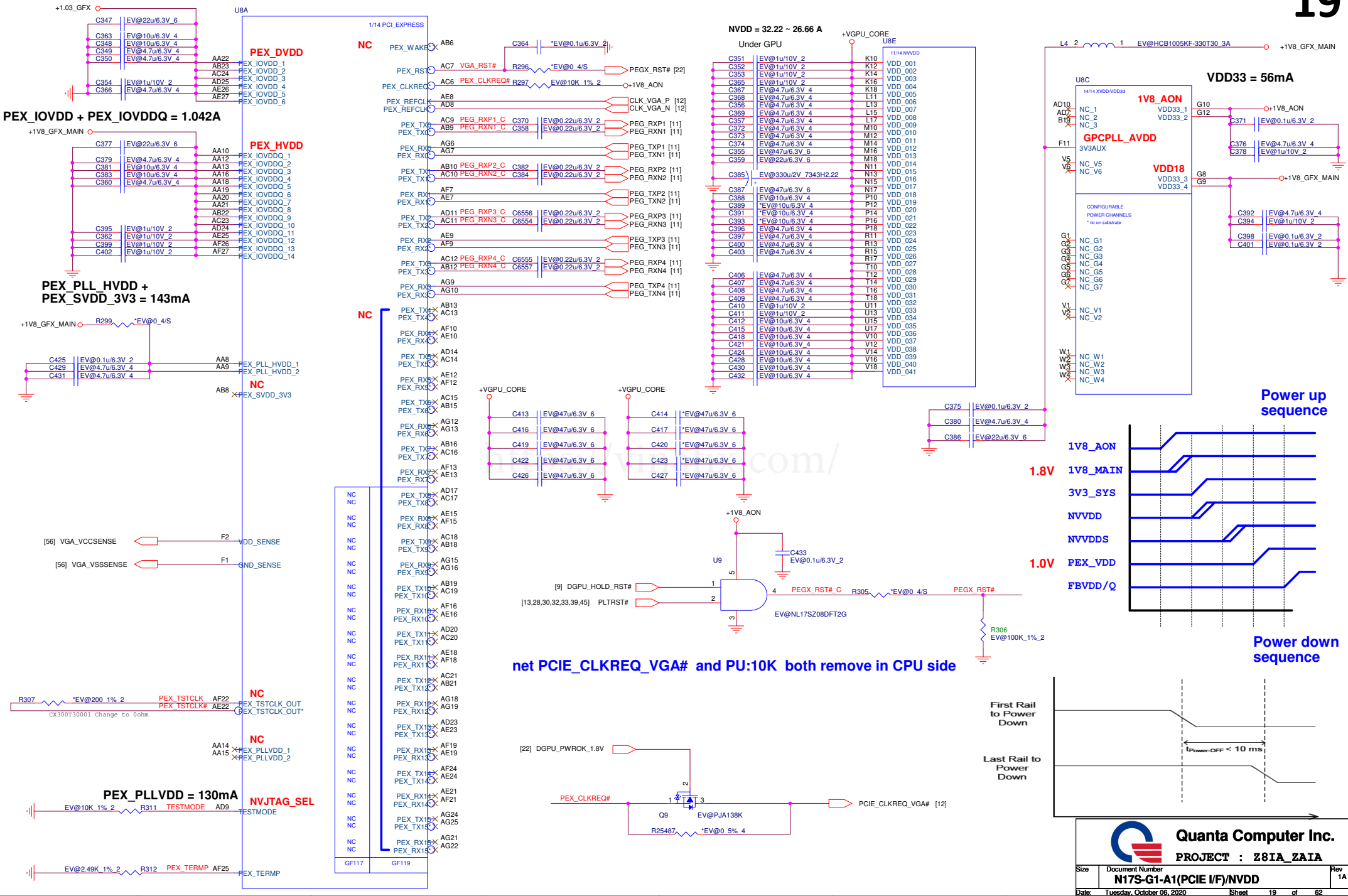

JDIM02A
DDR4 SODIMM 260 PIN
(260P)
JDIM02B
DDR4 SODIMM 260 PIN
(260P)
D4AR0-26001-1P40
D4AR0-26001-1P40
2.48A
0.5A
600mA
wide/spacing --> 20mils/20mils
VREF DQ0 M1 Solution
Follow reference
board DIMM1
SA0,1,2=LHL
Quanta Computer Inc.
PROJECT : Z8IA_ZAIA
DDR4 DIMM1-RVS(4.0H)
Tuesday, October 06, 2020


PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
Under GPU
VDD33 = 56mA
net PCIE_CLKREQ_VGA# and PU:10K both remove in CPU side
Power up sequence
Power down sequence
1V8_AON
1V8_MAIN
3V3_SYS
NVVDD
NVVDDS
PEX_VDD
FBVDD/Q
1.8V
1.0V
First Rail to Power Down
Last Rail to Power Down
tPower-OFF < 10 ms
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PROJECT : Z8IA_ZAIA
N17S-G1-A1(PCIE I/F)/NVDD
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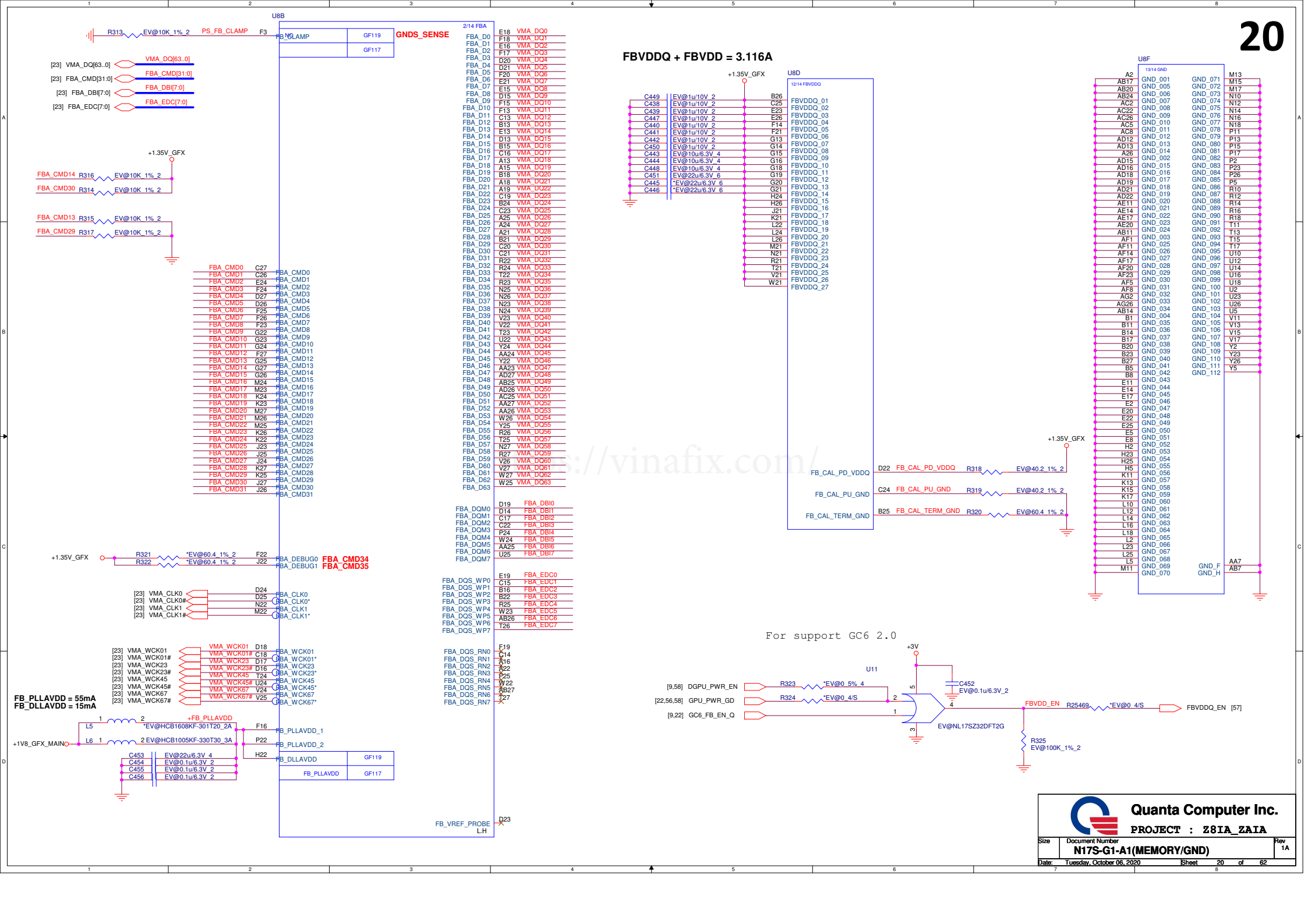

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Size	Document Number	Rev
	N17S-G1-A1(MEMORY/GND)	1A

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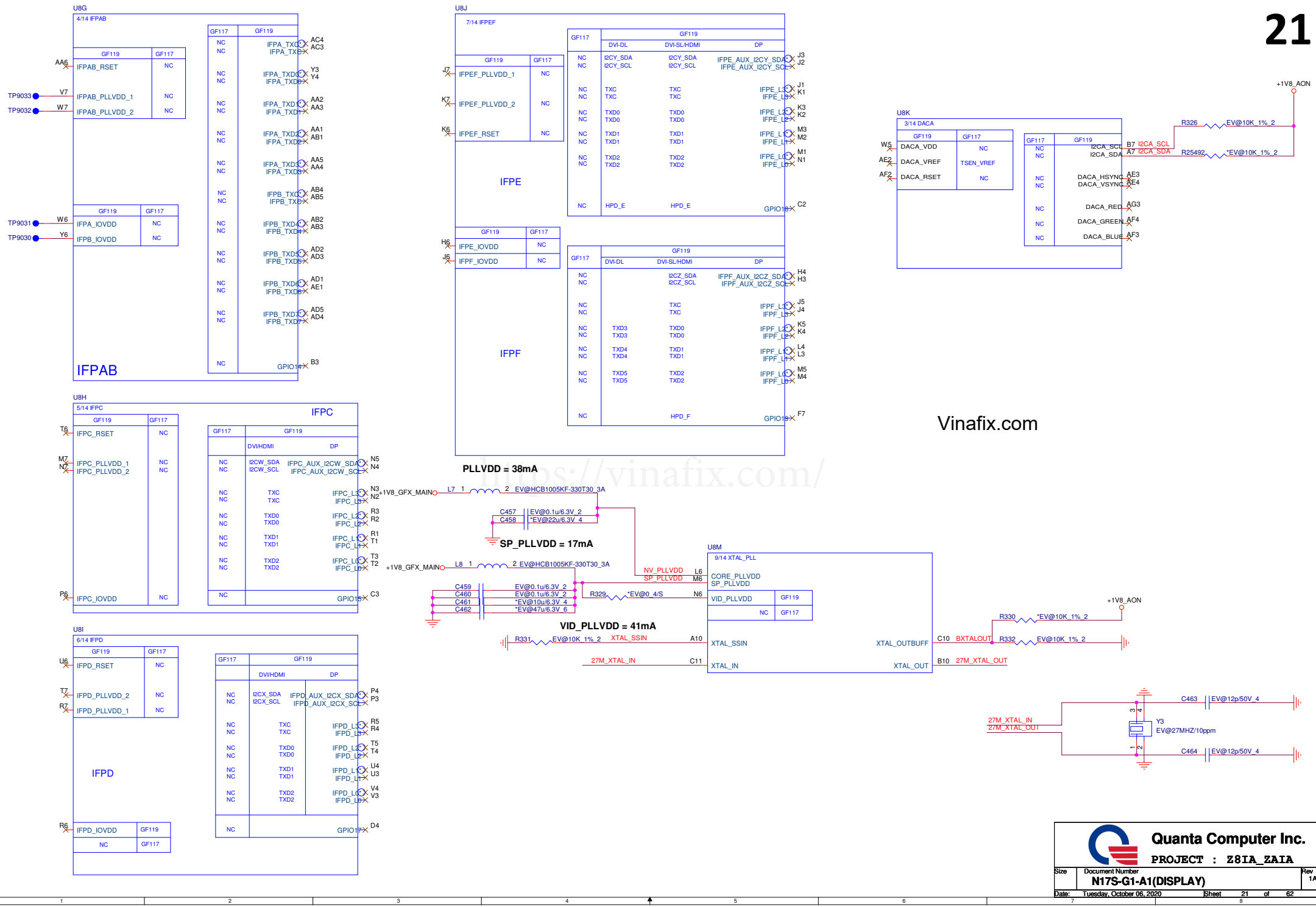
U8G
4/14 IFPAB
IFPAB
U8J
7/14 IFPEF
IFPE
IFPF
U8K
3/14 DACA
U8H
5/14 IFPC
IFPC
U8I
6/14 IFPD
IFPD
U8M
9/14 XTAL_PLL
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
+1V8_AON
+1V8_GFX_MAIN
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https://vinafix.com/
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N17S-G1-A1(DISPLAY)
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1A
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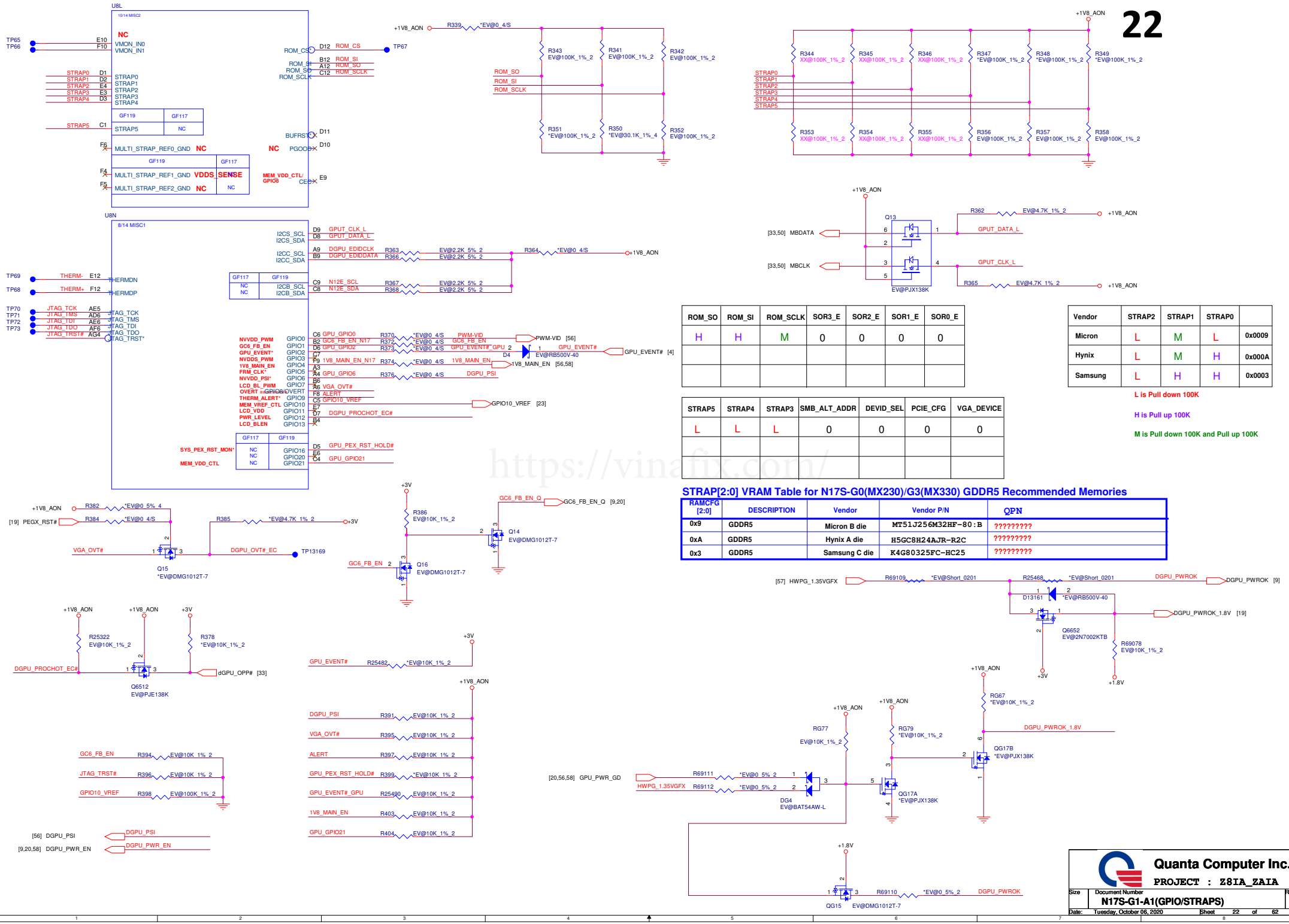

ROM_SO	ROM_SI	ROM_SCLK	SOR3_E	SOR2_E	SOR1_E	SOR0_E
H	H	M	0	0	0	0

Vendor	STRAP2	STRAP1	STRAP0	
Micron	L	M	L	0x0009
Hynix	L	M	H	0x000A
Samsung	L	H	H	0x0003

L is Pull down 100K

H is Pull up 100K

M is Pull down 100K and Pull up 100K

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

STRAP[2:0] VRAM Table for N17S-G0(MX230)/G3(MX330) GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	QPN
0x9	GDDR5	Micron B die	MT51J256M32HF-80:B	?????????
0xA	GDDR5	Hynix A die	H5GC8H24AJR-R2C	?????????
0x3	GDDR5	Samsung C die	K4G80325FC-HC25	?????????

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MF=0 Non-mirrored

Channel 0 <0-31>

MF=0 Non-mirrored

CHANNEL A: 2G/4G GDDR5

Channel 0 <32-63>

MF=0 Non-mirrored

QD24~31

QD16~23

QD8~15

QD0~7

QD40~47

QD32~39

QD56~63

QD48~55

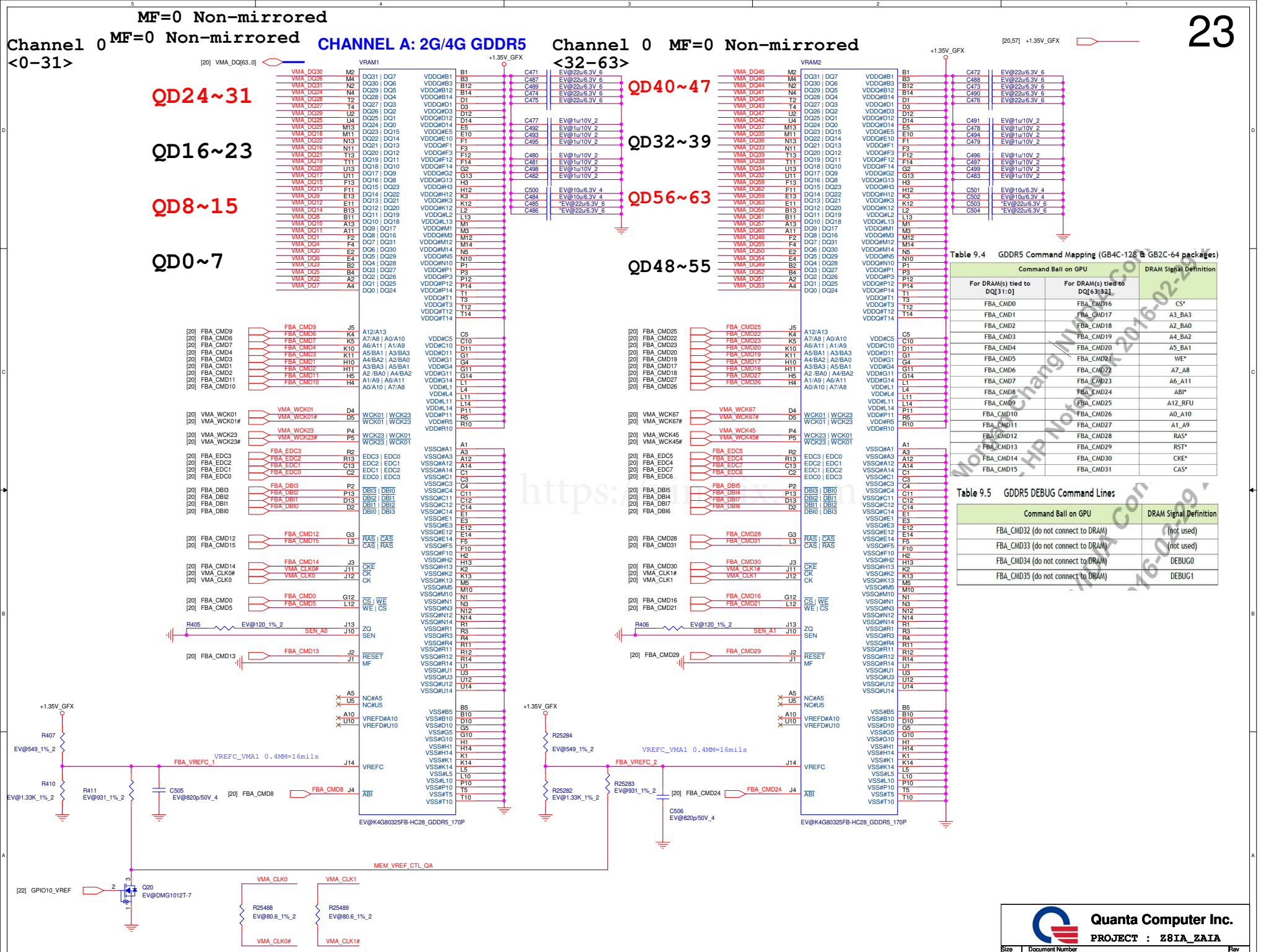

Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

Wang@HP Notebook 2016-02-29
Quanta Computer Inc. 2016-02-29

https://www.

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	N17S-G0-A1(GDDR5-1)	1A
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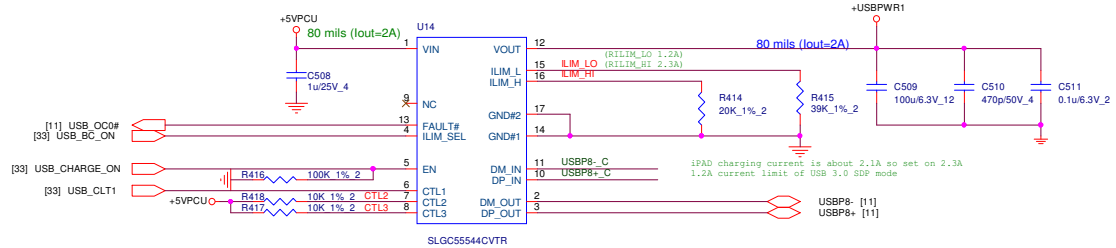
USB Charger to 3.0 (UBC)

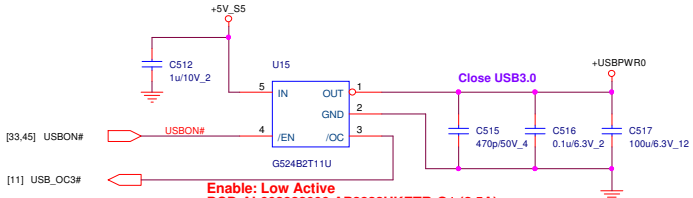


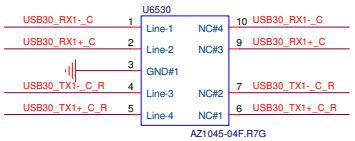
	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

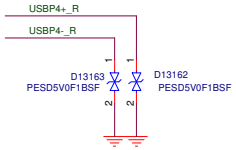
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

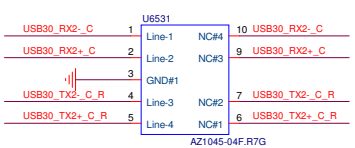
$$IOS_typ(mA) = 50{,}250/\{RILIM_XX(K\Omega)+0.1\}$$

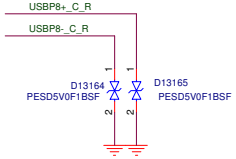
USB 3.0 Connector (UB3)

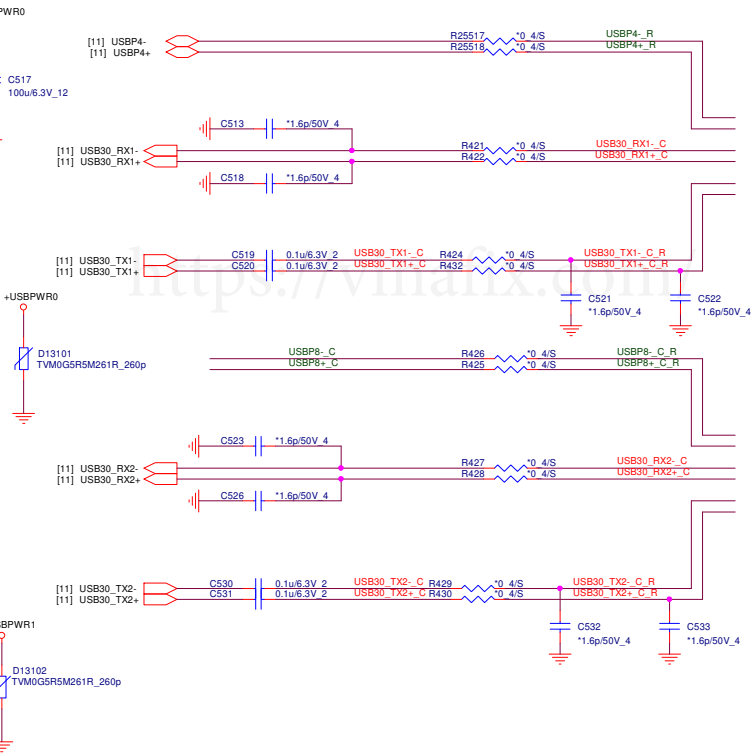


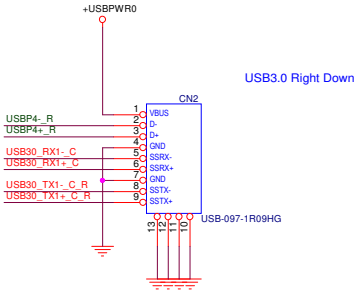


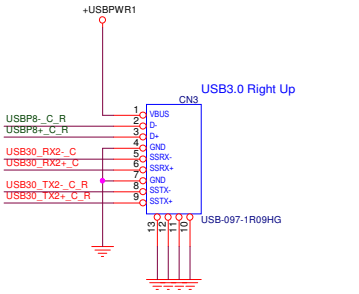












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	USB3.0*2/USB Chager*1		1A
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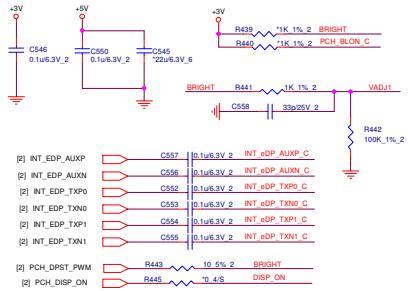
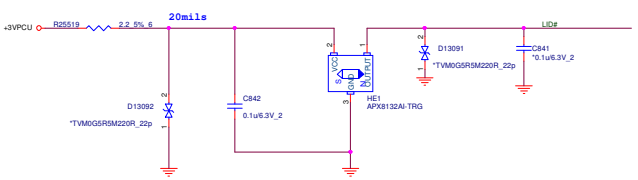
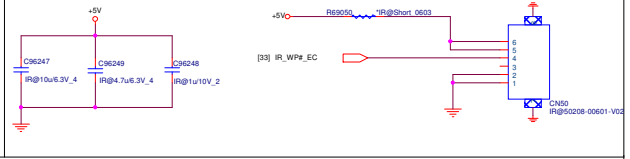


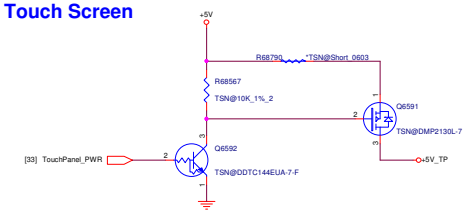
Hall Sensor



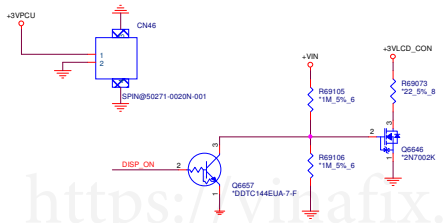
IR Camera



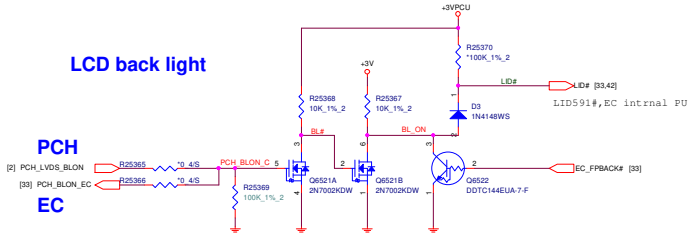
Touch Screen



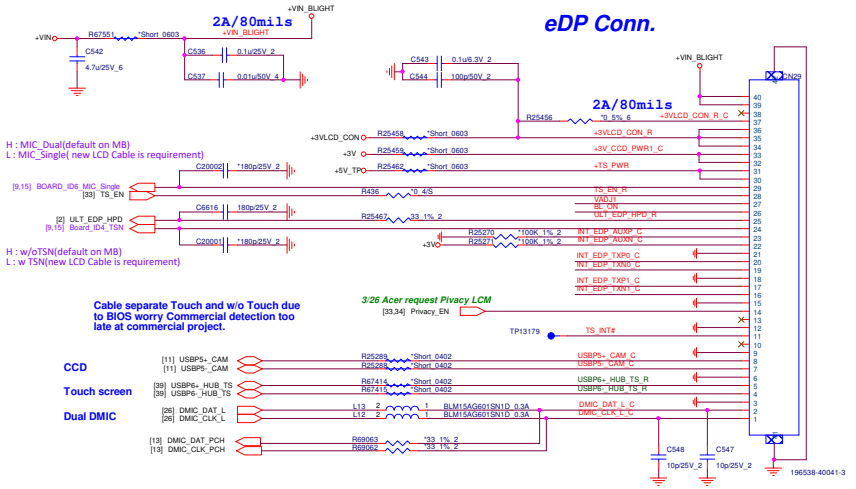
Stylus Pen charge

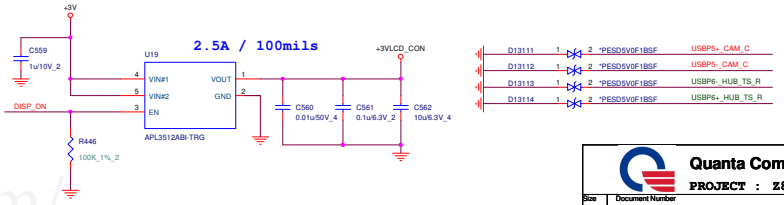


LCD back light



eDP Conn.





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Size	Document Number	Rev
	eDP/LID/CCD/TS/DMIC1/IR/Stylus	1A

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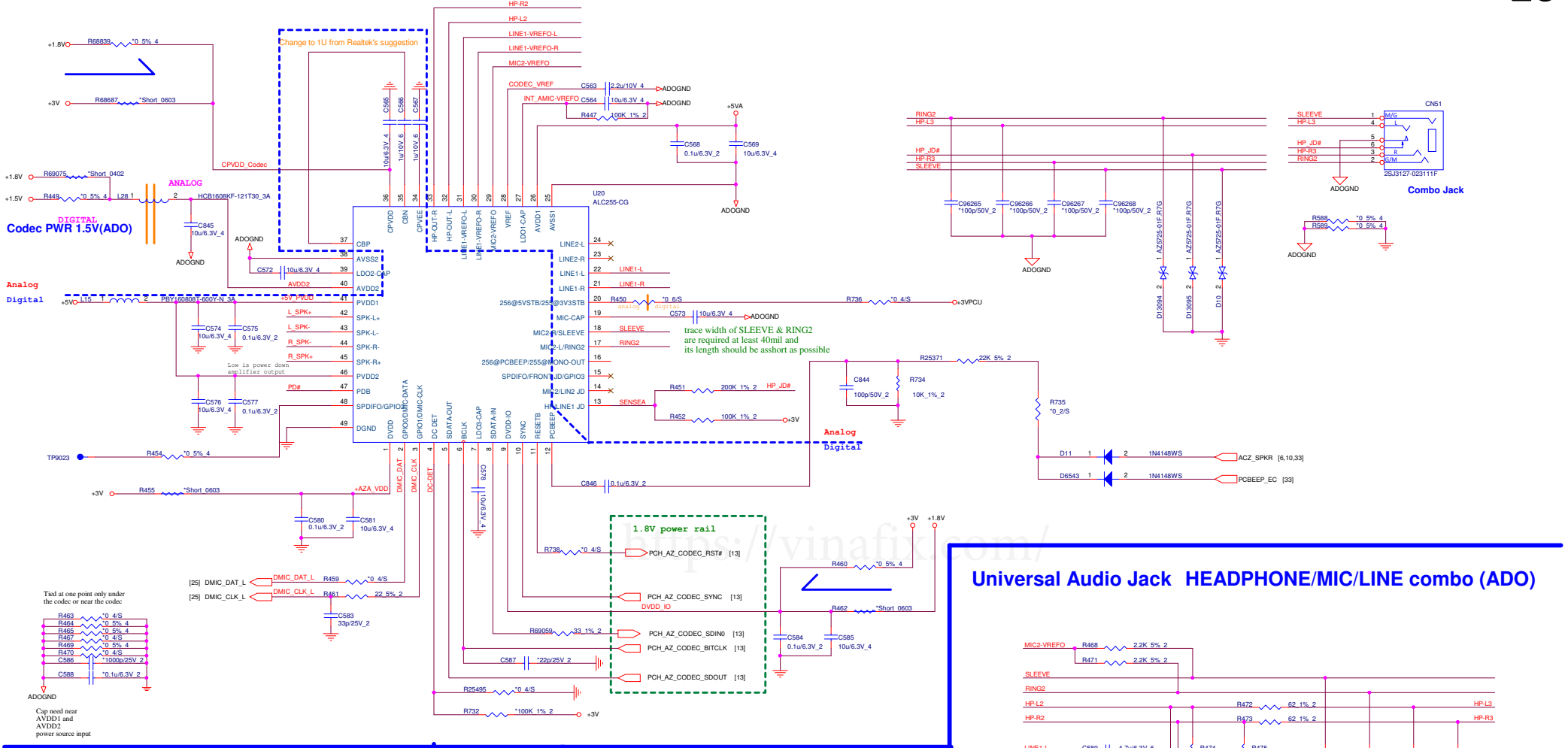
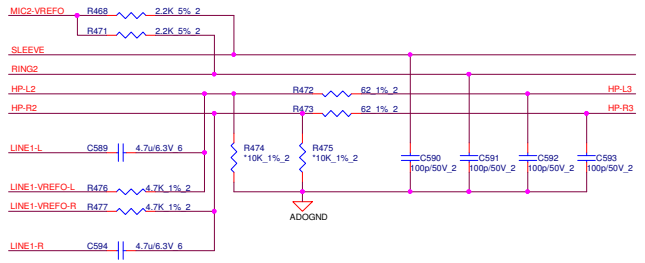
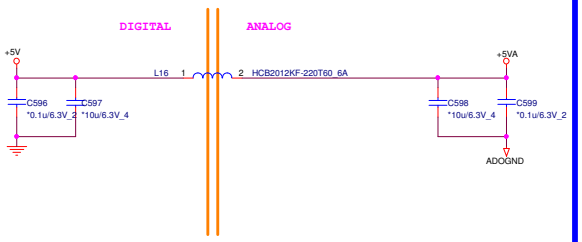
Codec(ADO)



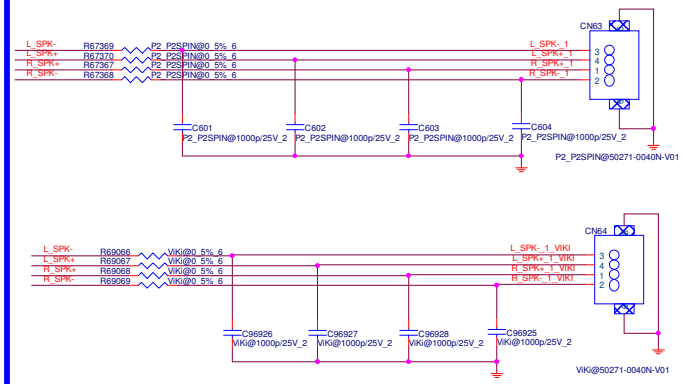
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



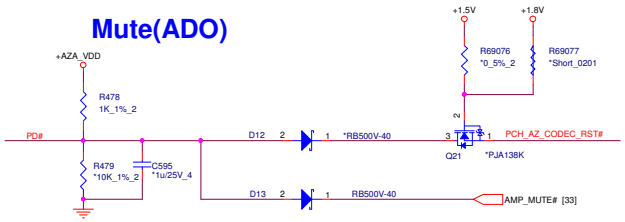
Codec PWR 5V(ADO)



Internal Speaker



Mute(ADO)



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Quanta Computer Inc.
PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	Audio Codec/HP/SPK	1A
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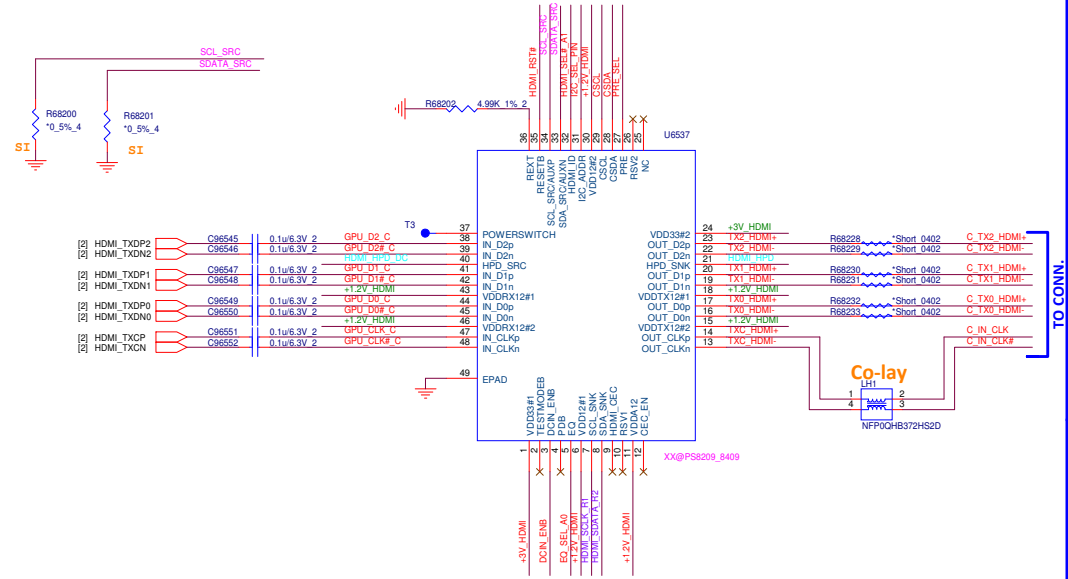
HDMI Retimer(HDM)

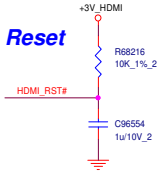


PS8409 strap pin

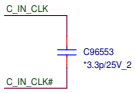
DCIN_ENB DC coupling enable; Internal pull up, 3.3V I/O. L: DC coupling input H: Default,AC coupling input	DCIN_ENB R68199 4.7K_1%_2
I2C_SEL_PIN I2C Slave Address selection; Internal pull down, 3.3V I/O. L: Default, Slave address 0x10-0x2F. H: Alternative salve address 0x90-0x9F, 0xD0-0xDF.	+3V_HDMI R68203 *4.7K_1%_2 I2C_SEL_PIN
HDMI_SEL#_A1 HDMI_ID enable ; Internal pull down , 3.3V I/O. L: Default, HDMI ID enable H: HDMI ID disable	+3V_HDMI R68204 *4.7K_1%_2 HDMI_SEL#_A1
EQ_SEL_A0 Receiver equalization setting; Internal pull up , 3.3V I/O. L: Compensaton for channel loss up to 13dB H: Default , Compensation for channel loss up to 17dB M: Compensation for channel loss up to 11dB	EQ_SEL_A0 +3V_HDMI R68210 *4.7K_1%_2 R68211 *4.7K_1%_2
PRE_SEL Output pre-emphasis setting; Internal pull up, 3.3V I/O. L: Pre-emphasis =2.5dB H: Default, No Pre-emphasis	PRE_SEL R68215 *4.7K_1%_2

MSIC

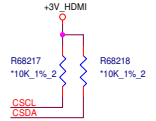
Reset



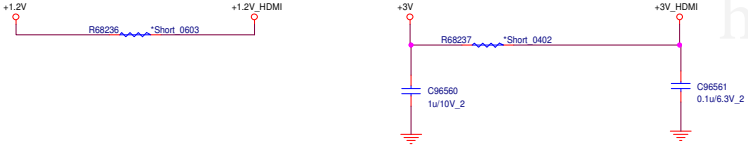
Reserve



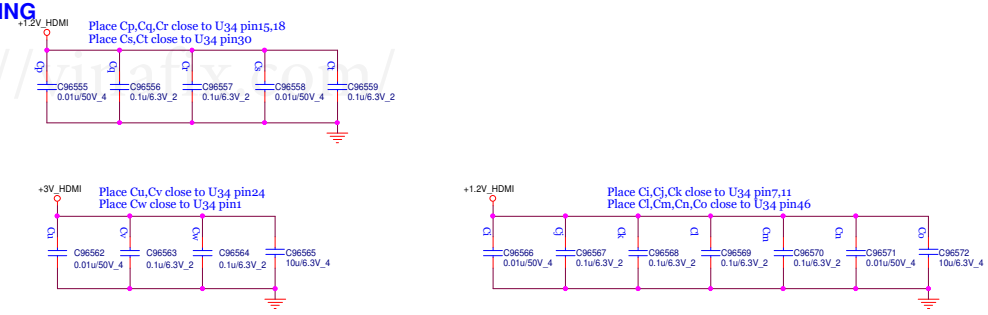
Optional



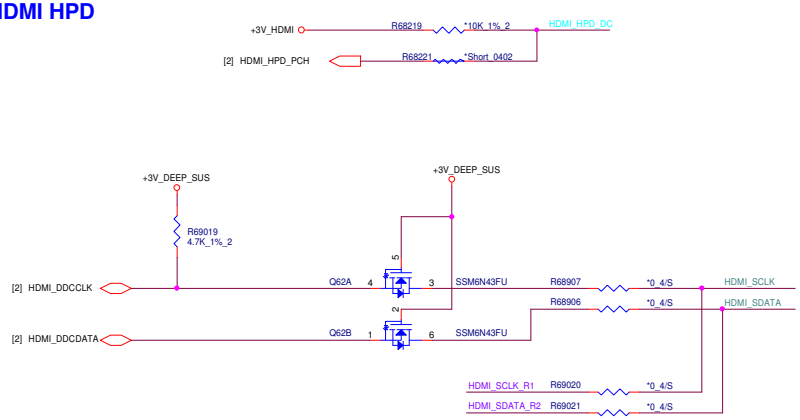
POWER



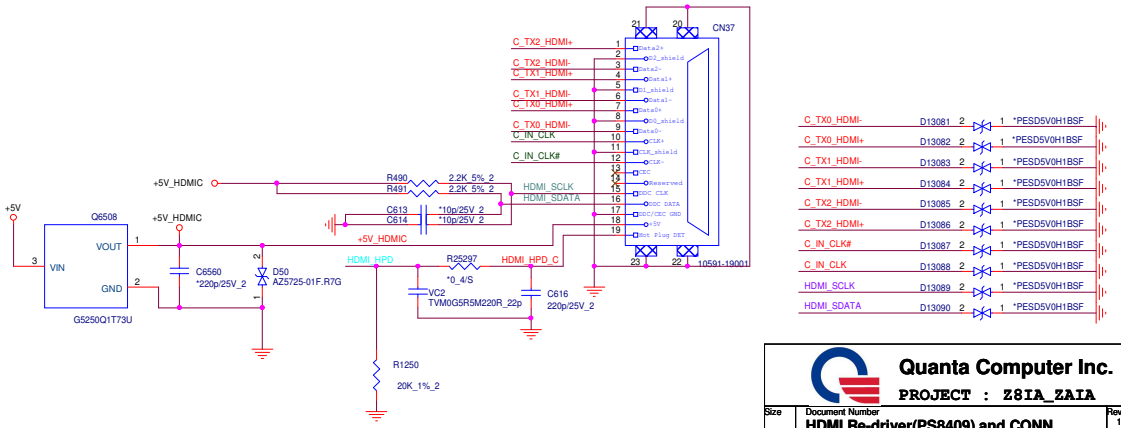
DECOUPLING



HDMI HPD



CONNECTOR



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Size	Document Number	Rev
	HDMI Re-driver(PS8409) and CONN	1A
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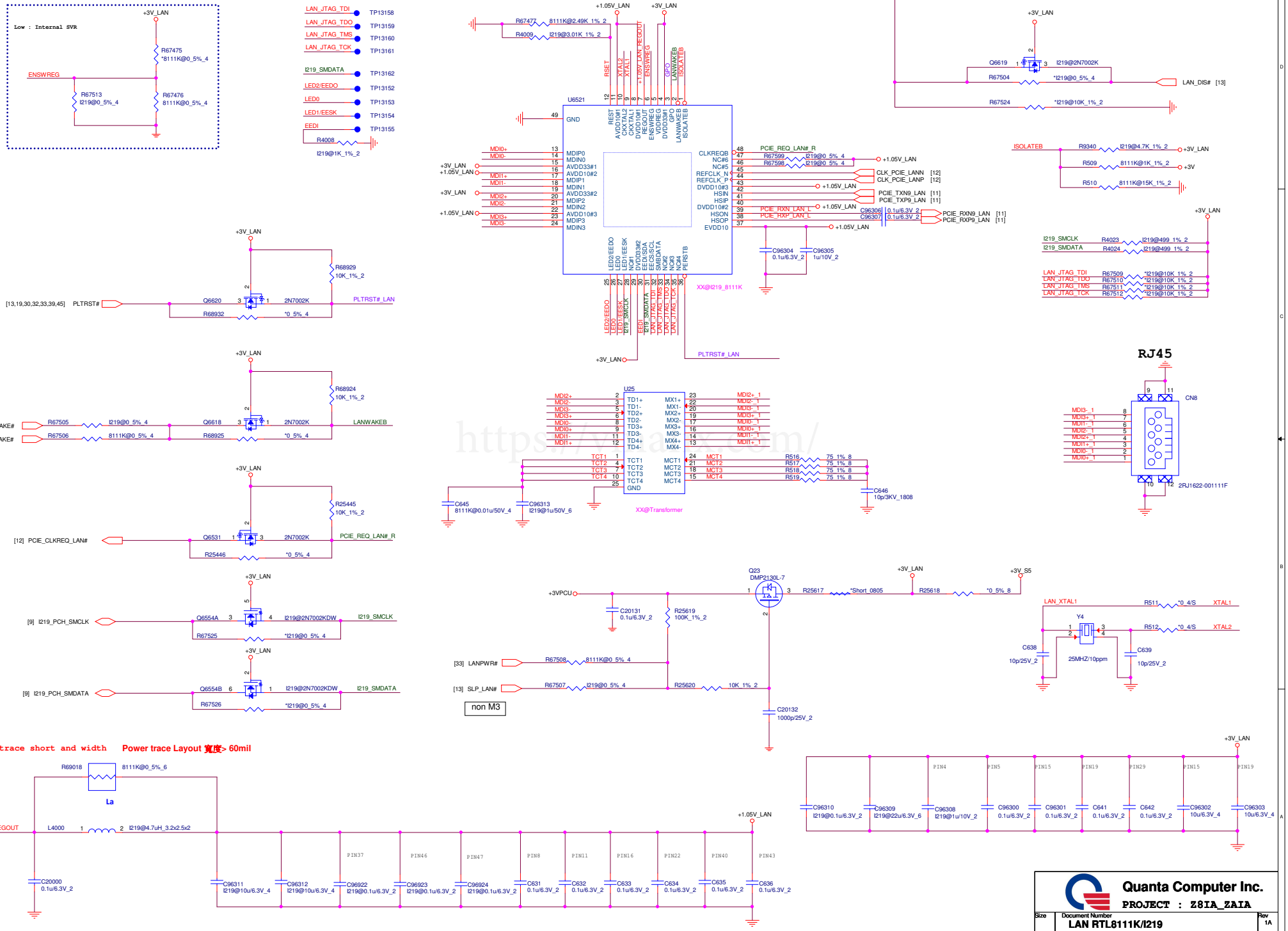
LAN RTL8111K-CG/Intel I219



https://www.[illegible].com/

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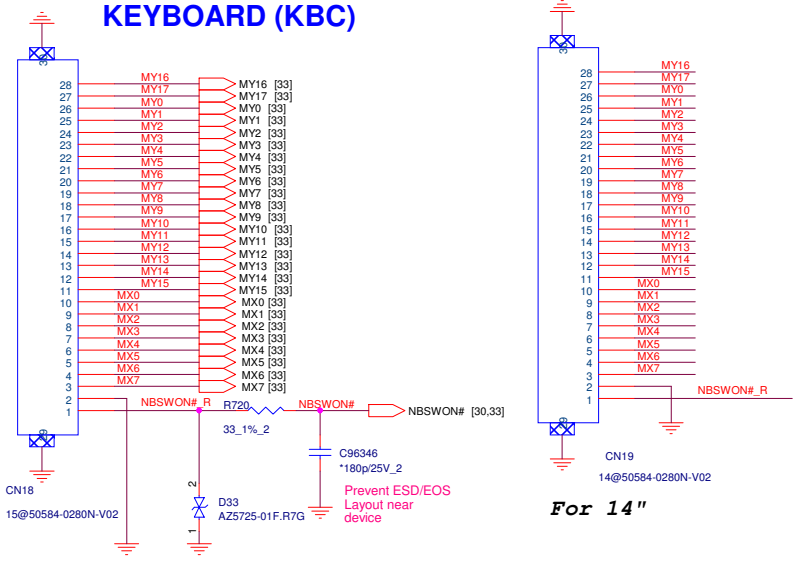
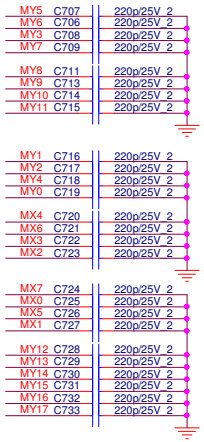
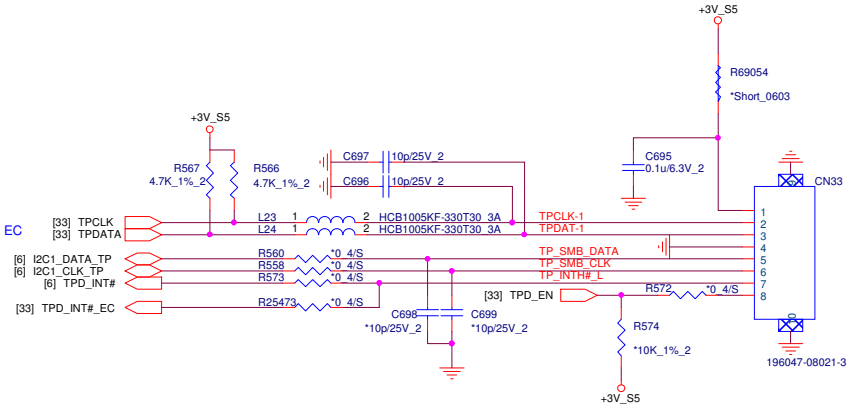
Size	Document Number	Rev
	LAN RTL8111K/I219	1A
Date: Tuesday, October 06, 2020	Sheet 28 of 62	

KEYBOARD (KBC)

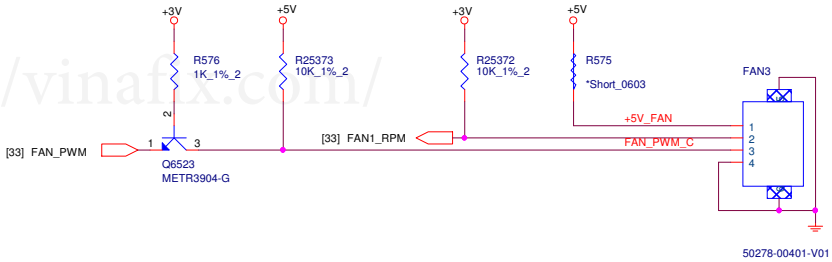




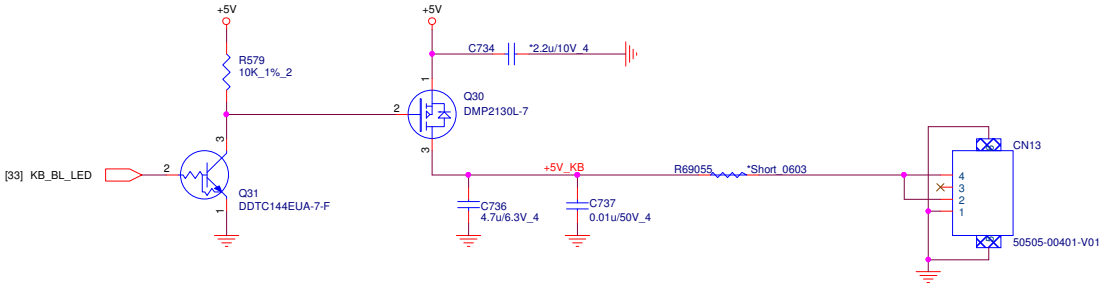
Touch Pad



FAN



KB_BL LED



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Quanta Computer Inc.

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Size	Document Number	Rev
	KB/TP/FAN/PB/KBL	1A
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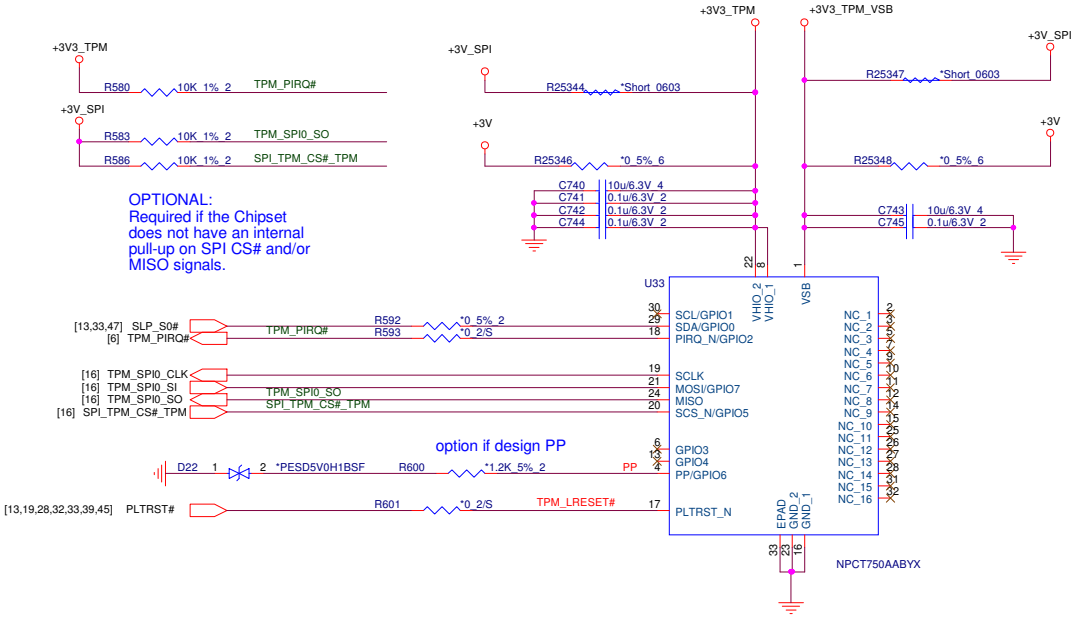
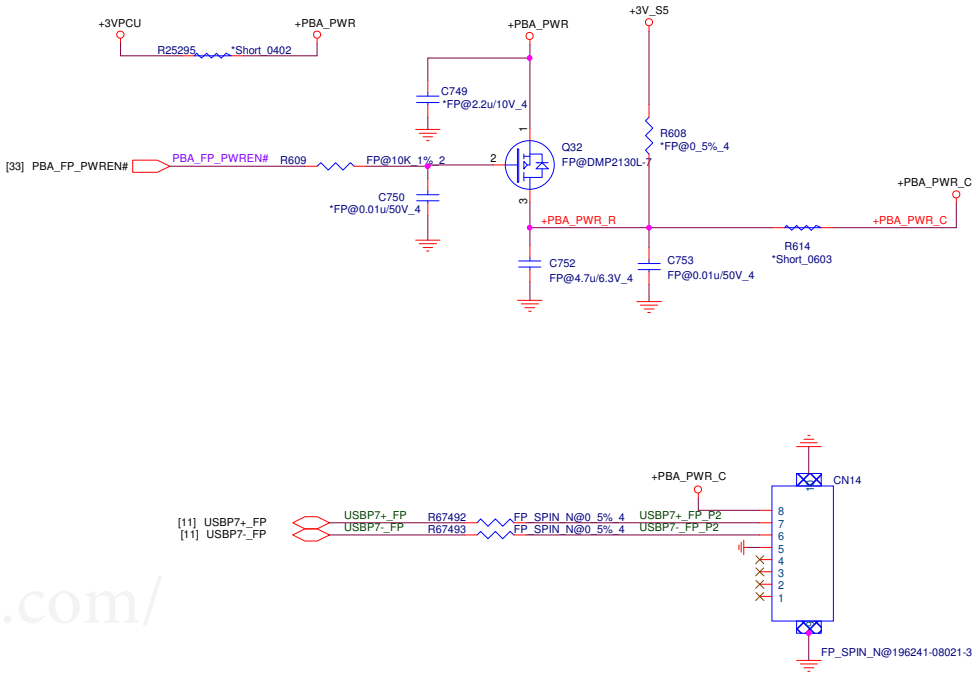
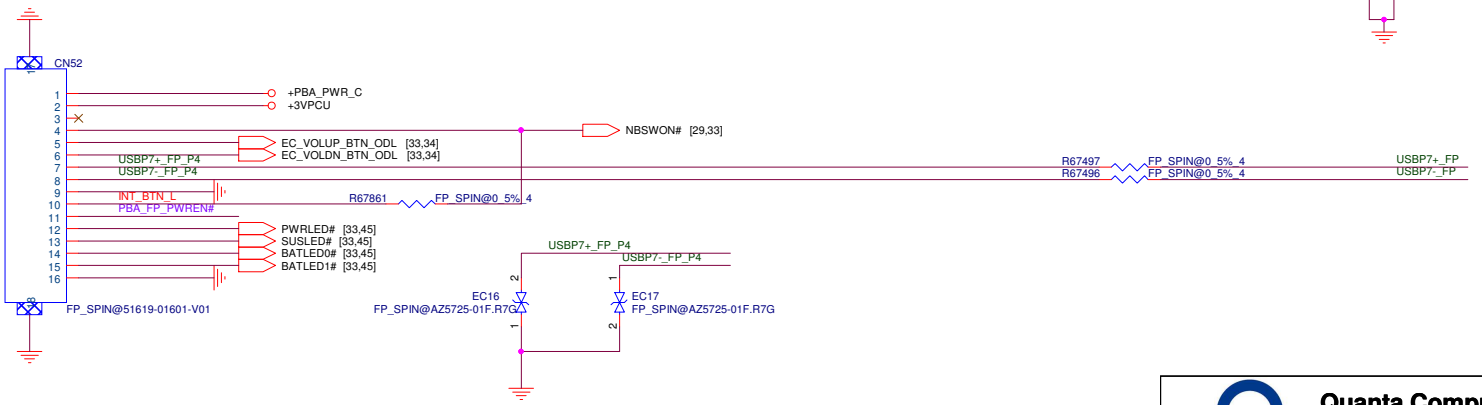
TPM NPCT750



Finger print



Reserve for SPIN



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Quanta Computer Inc.

PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	TPM/PBA/Spin side key	1A

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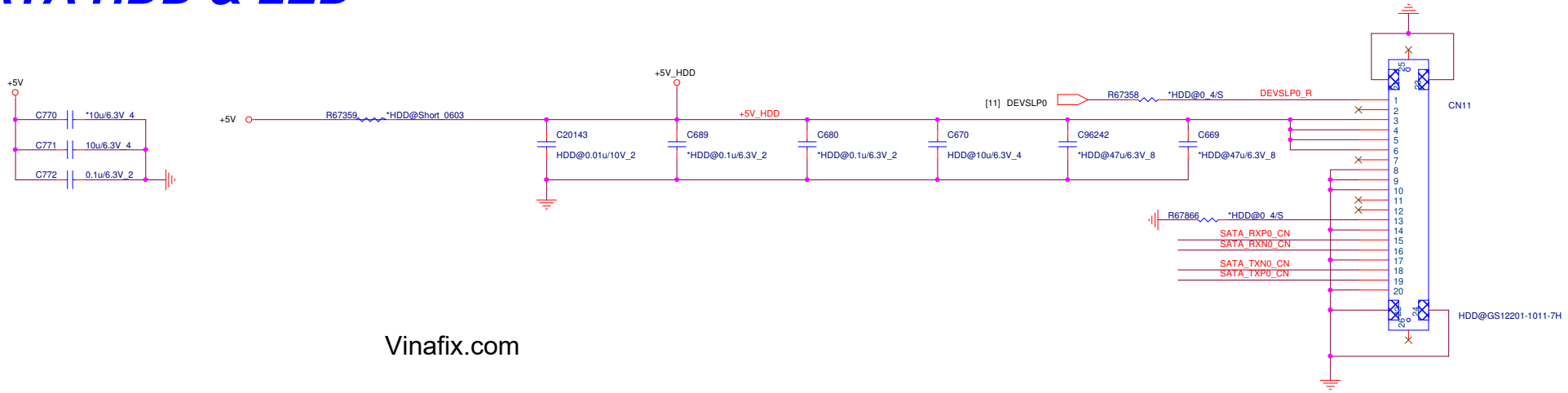
SATA HDD & LED



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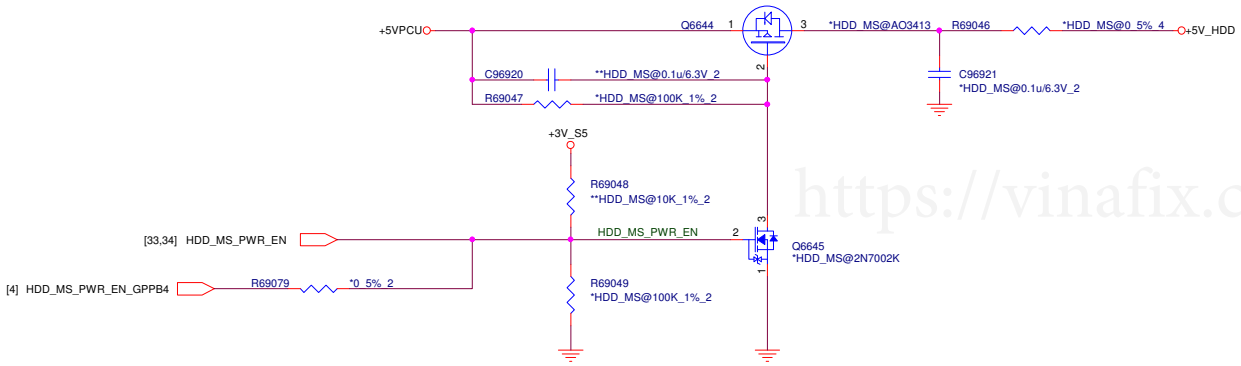
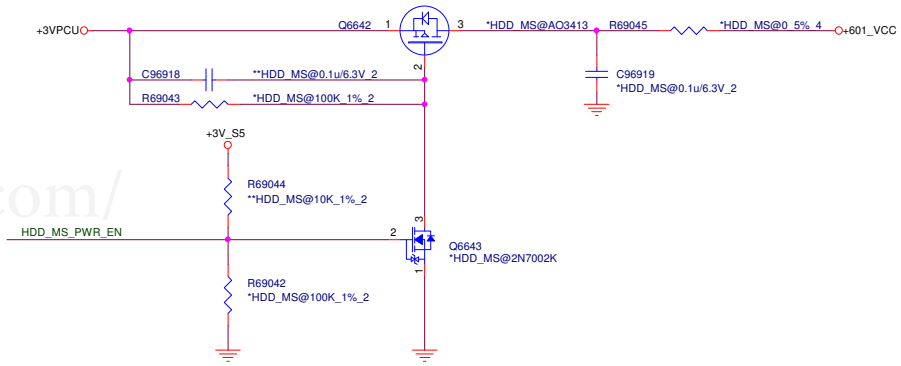
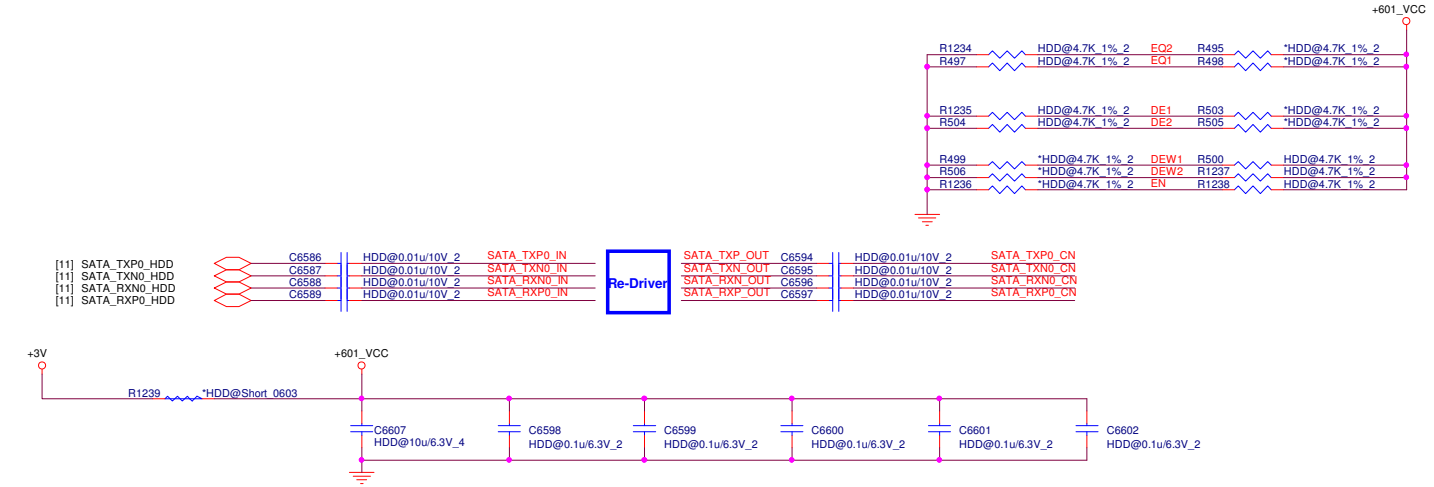
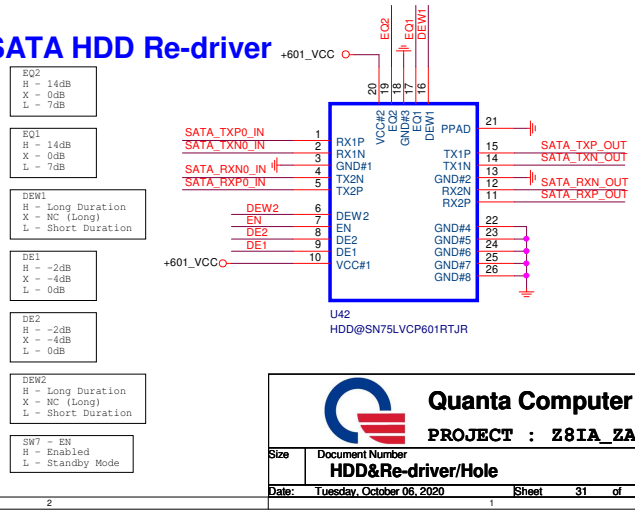


https://vinafix.com/





SATA HDD Re-driver



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Size	Document Number	Rev
	HDD&Re-driver/Hole	1A

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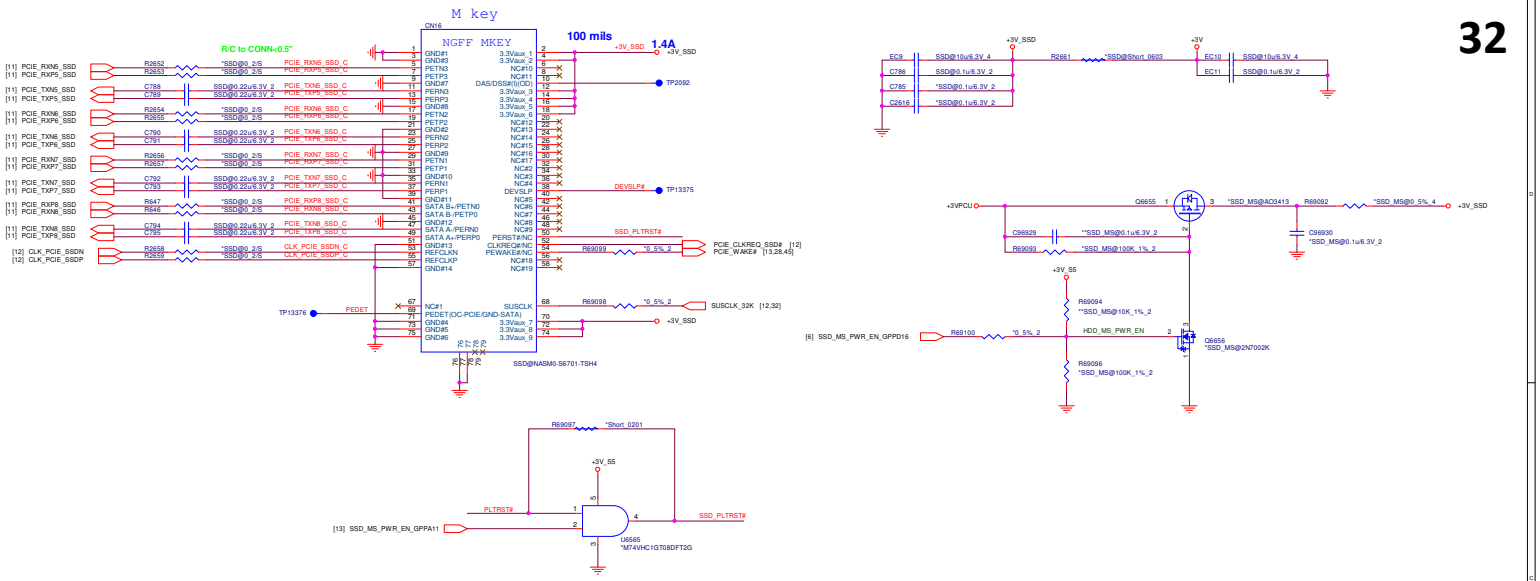
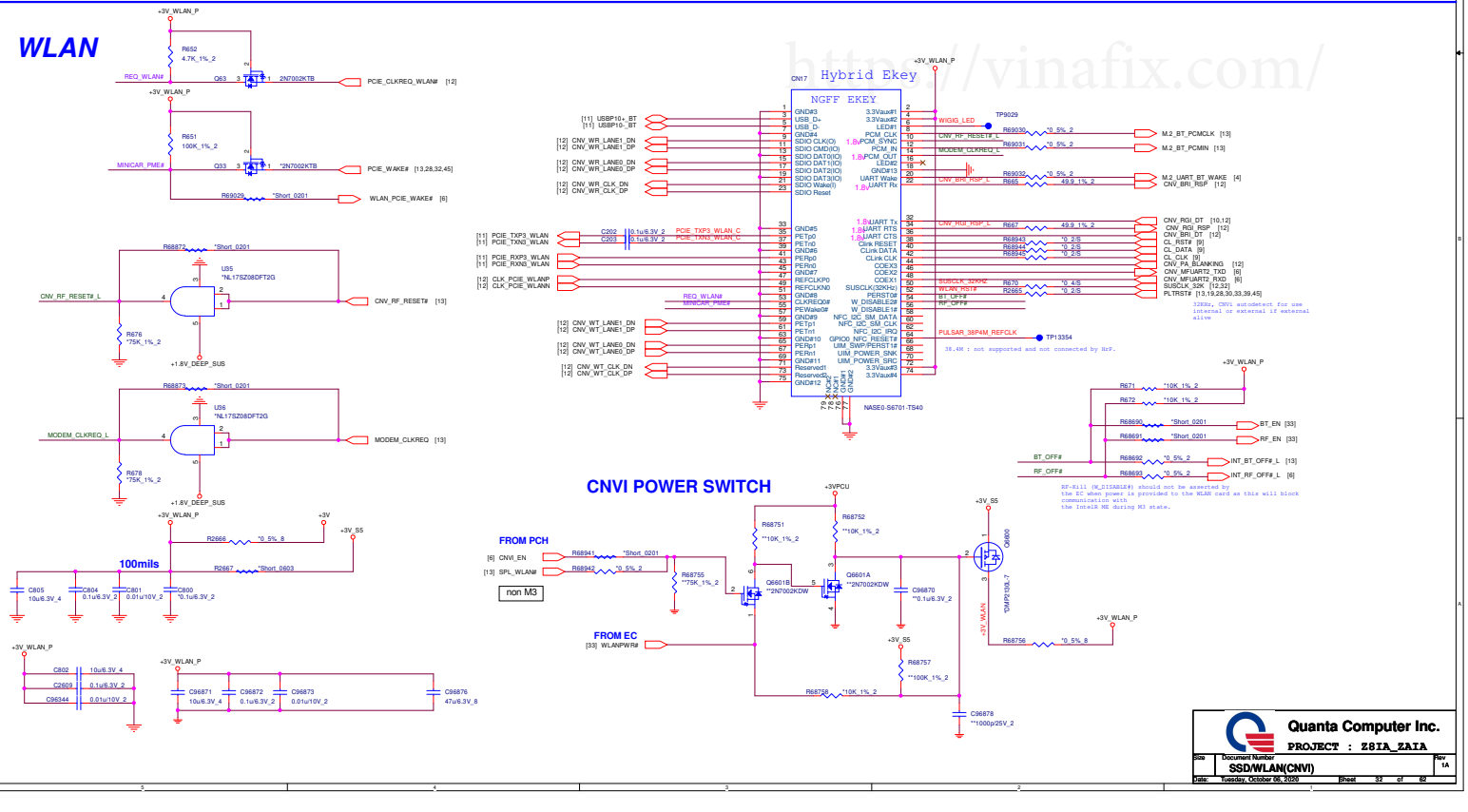

M key
CN16
NGFF MKEY
R/C to CONN<0.5"
100 mils
1.4A
+3V_SSD
TP2092
DEVSLP#
TP13375
SSD_PLTRST#
PCIE_CLKREQ_SSD# [12]
PCIE_WAKE# [13,28,45]
SUSCLK_32K [12,32]
TP13376
PEDET
SSD@NASM0-S6701-TSH4
R69097 *Short_0201
+3V_S5
PLTRST#
SSD_PLTRST#
[13] SSD_MS_PWR_EN_GPPA11
U6565
*MT4VHC1GT08DFT2G

+3V_SSD
R2661 *SSD@Short_0603
+3V
+3VPCU
Q6655 *SSD_MS@AO3413
R69092 *SSD_MS@0.5%_4
C96929 **SSD_MS@0.1u/6.3V_2
R69093 *SSD_MS@100K_1%_2
C96930 *SSD_MS@0.1u/6.3V_2
R69094 **SSD_MS@10K_1%_2
HDD_MS_PWR_EN
Q6656 *SSD_MS@2N7002K
R69096 *SSD_MS@100K_1%_2
[6] SSD_MS_PWR_EN_GPPD16
R69100 *0.5%_2


WLAN
+3V_WLAN_P
REQ_WLAN#
Q63 2N7002KTB
PCIE_CLKREQ_WLAN# [12]
MINICAR_PME#
Q33 *2N7002KTB
PCIE_WAKE# [13,28,32,45]
R69029 *Short_0201
WLAN_PCIE_WAKE# [6]
R68872 *Short_0201
U35
*NL17SZ08DFT2G
CNV_RF_RESET# [13]
+1.8V_DEEP_SUS
R68873 *Short_0201
U36
MODEM_CLKREQ [13]
CNVI POWER SWITCH
FROM PCH
[6] CNVI_EN
[13] SPL_WLAN#
non M3
FROM EC
[33] WLANPWR#
Q6601B *2N7002KDW
Q6601A *2N7002KDW
Q6600 *DMP2053L-7
100mils
CN17 Hybrid Ekey
NGFF EKEY
TP9029
TP13354
PLTSAR_38P4M_REFCLK
NASE0-S6701-TS40
BT_EN [33]
RF_EN [33]
INT_BT_OFF#_L [13]
INT_RF_OFF#_L [6]
BT_OFF#
RF_OFF#
Quanta Computer Inc.
PROJECT : Z8IA_ZAIA
SSD/WLAN(CNVI)
Tuesday, October 06, 2020
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EC(KBC)

IT5571 LQFP

U37 IT5571E-128/DX

LPC / eSPI
GPIO
CIR
UART port
WAKE UP
PWM
EXTERNAL SERIAL FLASH
A/D D/A
SPI ENABLE
KBMX
CLOCK
SM BUS
PS/2

11/11 FAE suggestion pin106 +3V_RTC change to +3VPCU_EC

12 mils

Prevent ESD/EOS Layout near device

Prevent ESD/EOS Layout near EC

EC Mirror Code
GPG2 PU 10K
GPD2 PD 100K (PCH side)

SM Bus 1	Battery , GPU
SM Bus 2	PD-CCG5 ,ThemalIC-98H ,ThemalIC-9AH ,Extension IO-IT8013
SM Bus 3	
SM Bus 4	

LED

SM BUS PU(KBC)

Battery module

UMA& VGA SKU
Need Stuff

CCG5

HWPG(KBC)

Reserve switch for test (MP remove)

Reset SW (FSW)

Debug port

https://

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Size	Document Number	Rev
	KBC IT5571	1A

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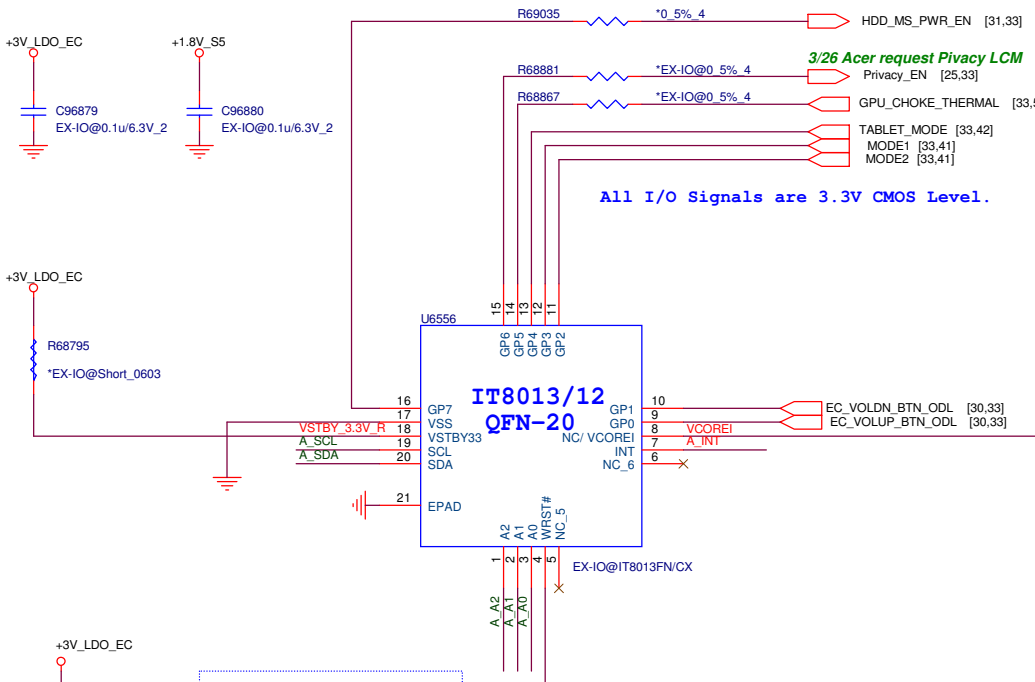
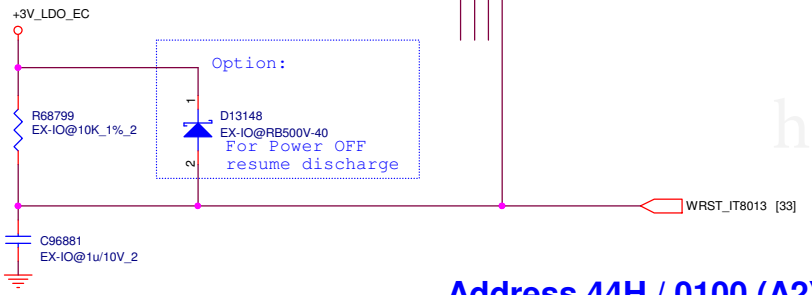


VSTBY_1.8V for IT8012

IT8013 / IT8012 difference

DEVICE	PIN8	PIN18
IT8013	NC	VSTBY33
IT8012	VCOREI	VSTBY33

Note:VCOREI power-up can't slow than VSTBY_3.3V.



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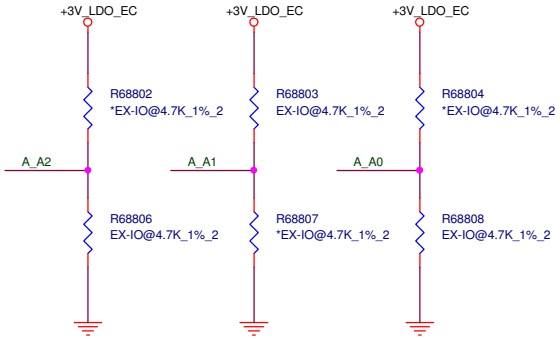
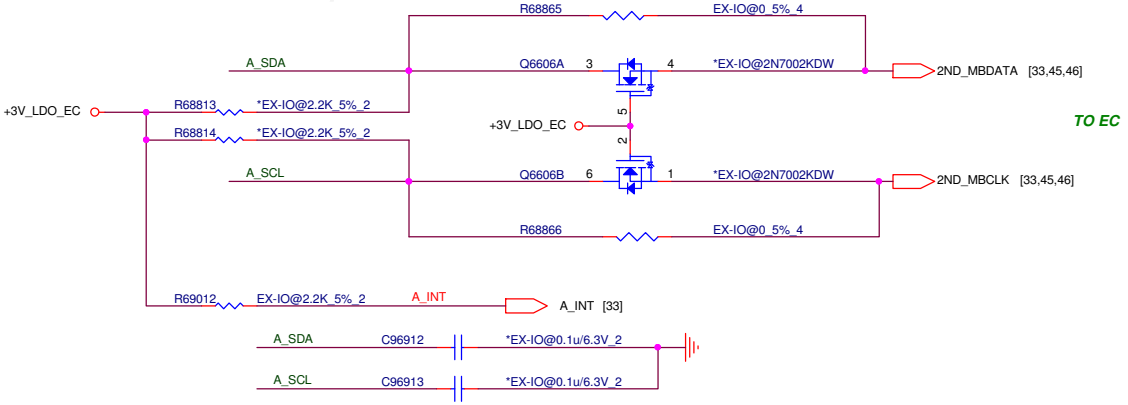
https://vinafix.com/

Address 44H / 0100 (A2)(A1)(A0)





Quanta Computer Inc.

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Size	Document Number	Rev
	USB DB/RS232/DMIC2	1A

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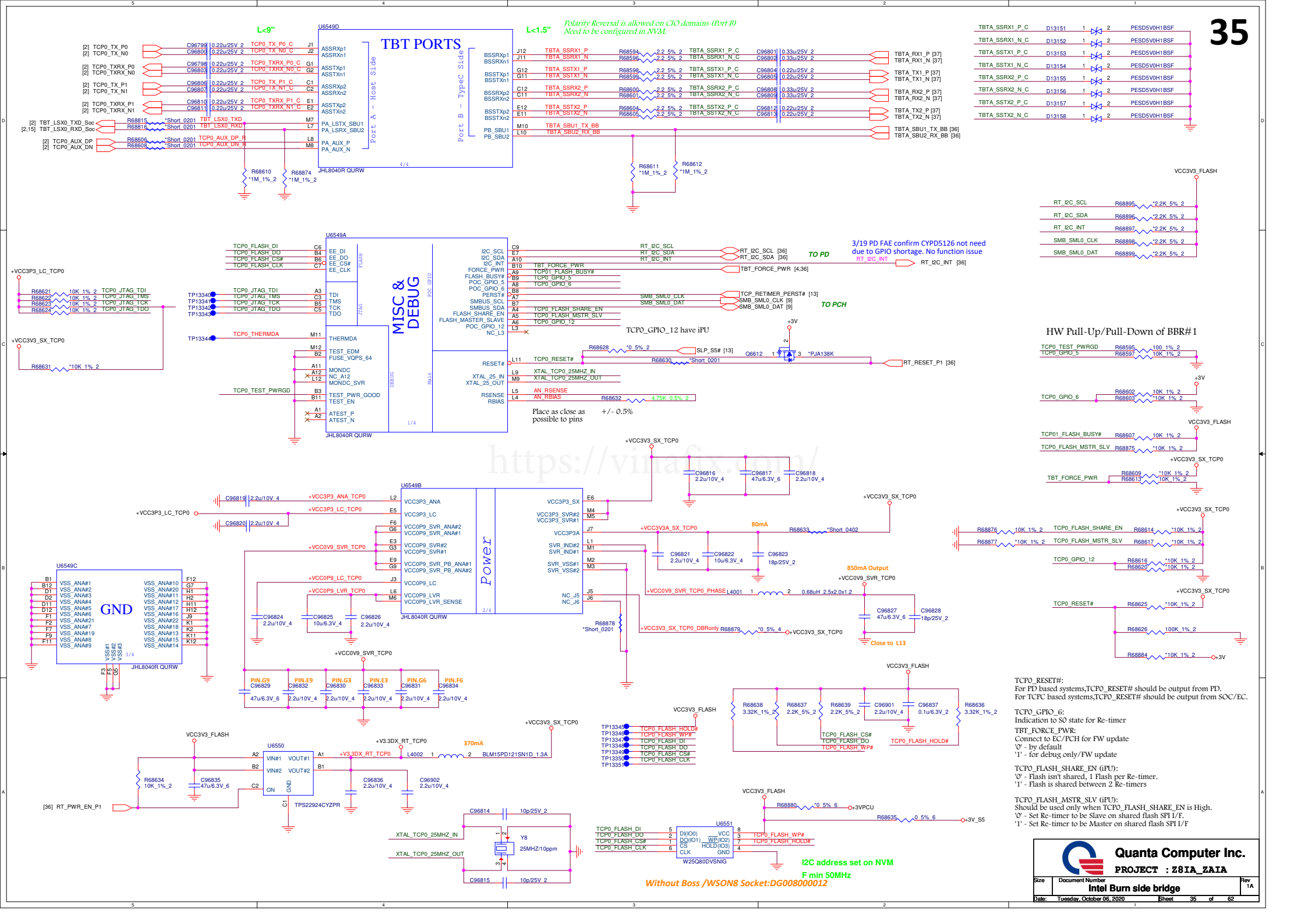

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Quanta Computer Inc.
PROJECT : Z8IA_ZAIA
Size | Document Number: Intel Burn side bridge | Rev: 1A
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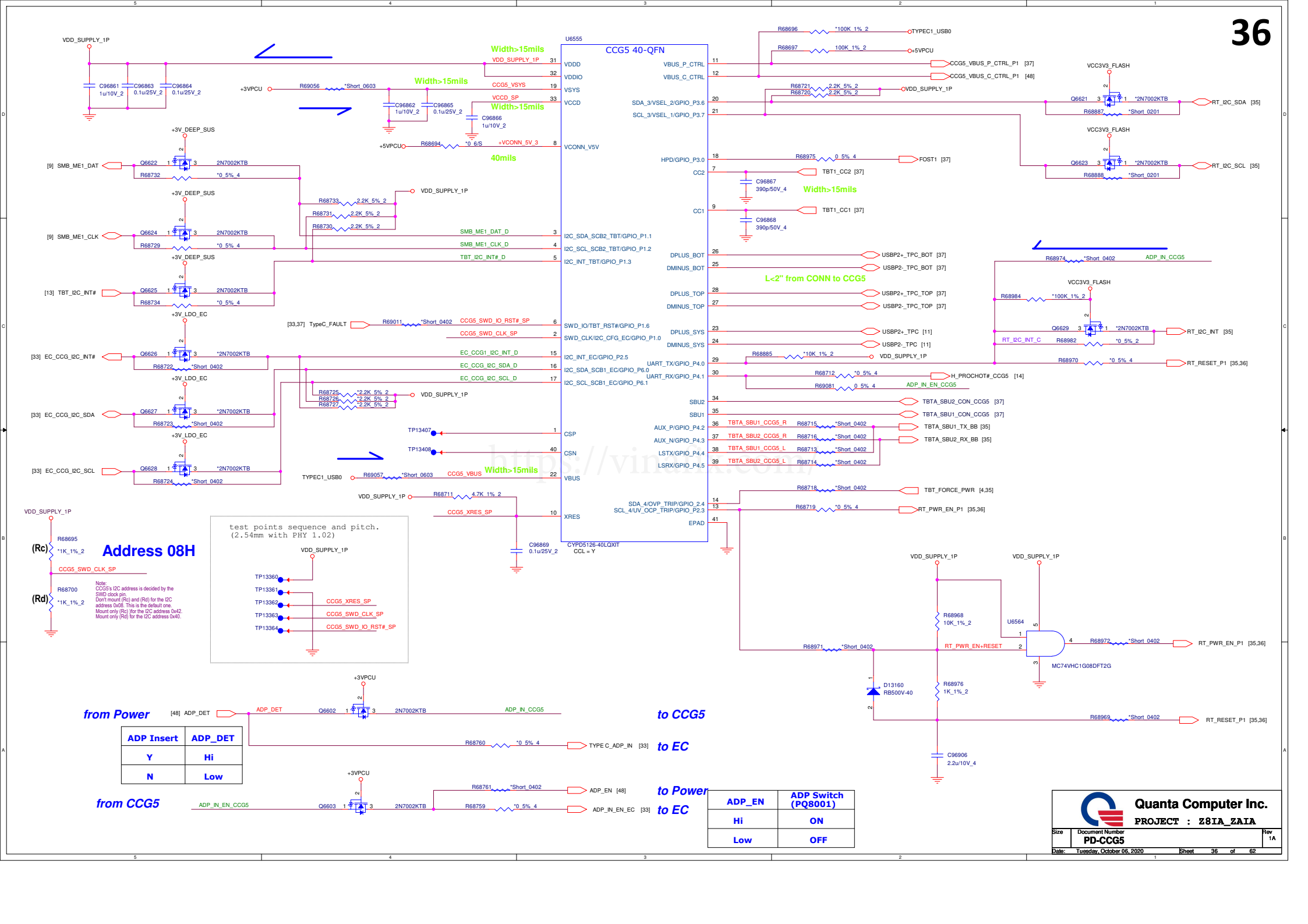

ADP Insert	ADP_DET
Y	Hi
N	Low

ADP_EN	ADP Switch (PQ8001)
Hi	ON
Low	OFF

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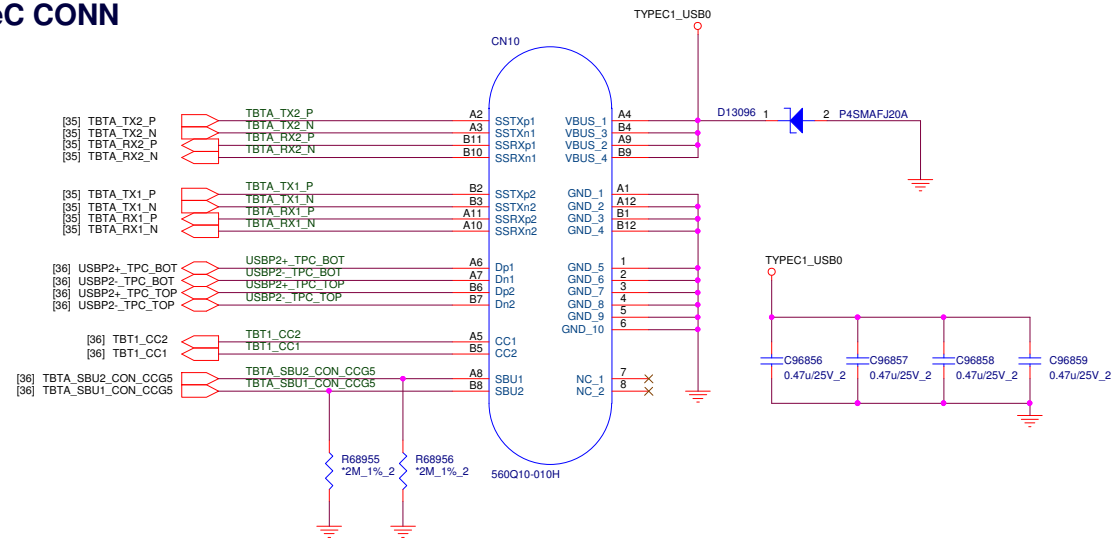
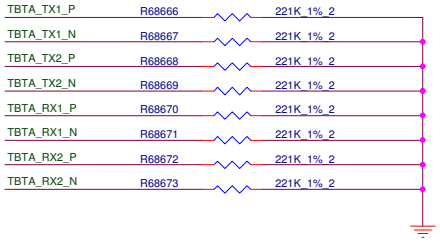
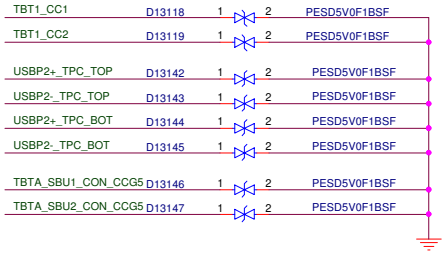
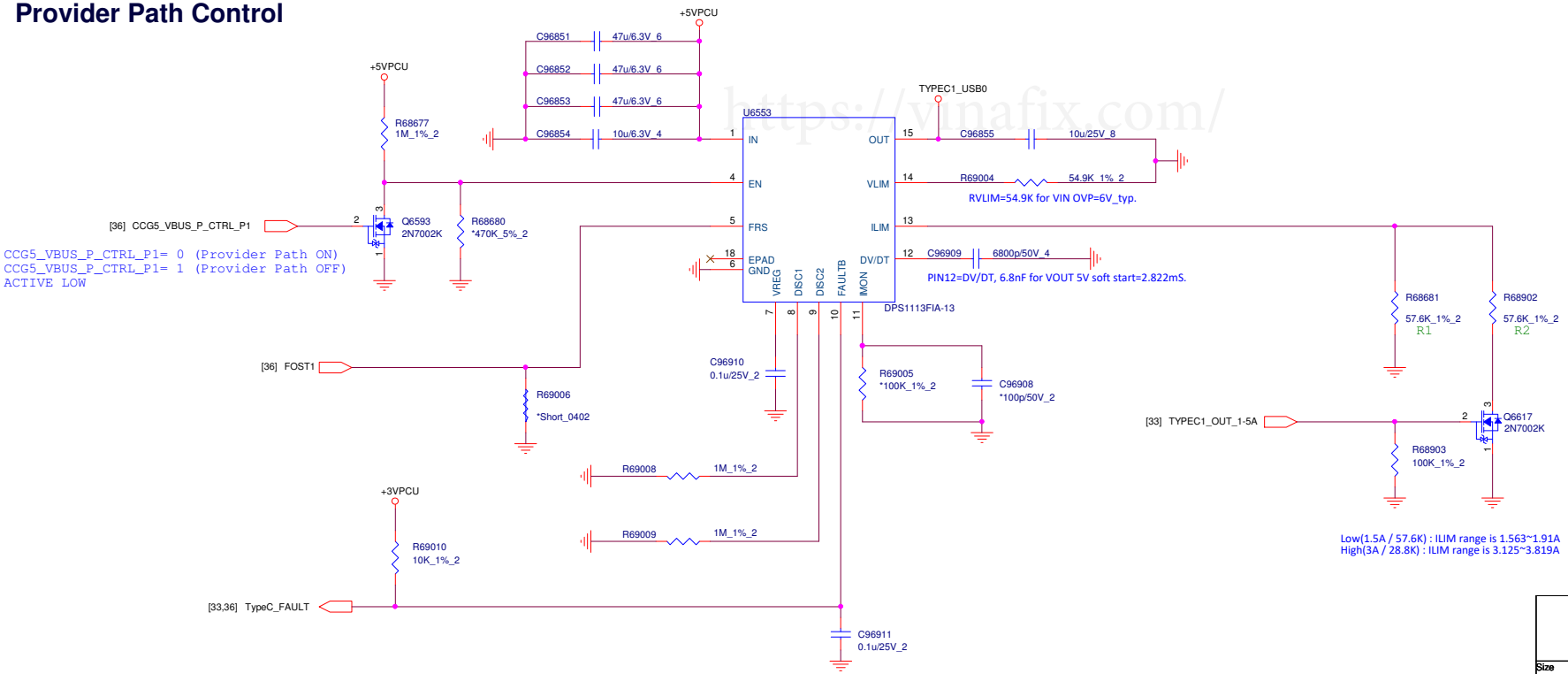
TypeC CONN







Provider Path Control



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Quanta Computer Inc.
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	TypeC CONN	1A
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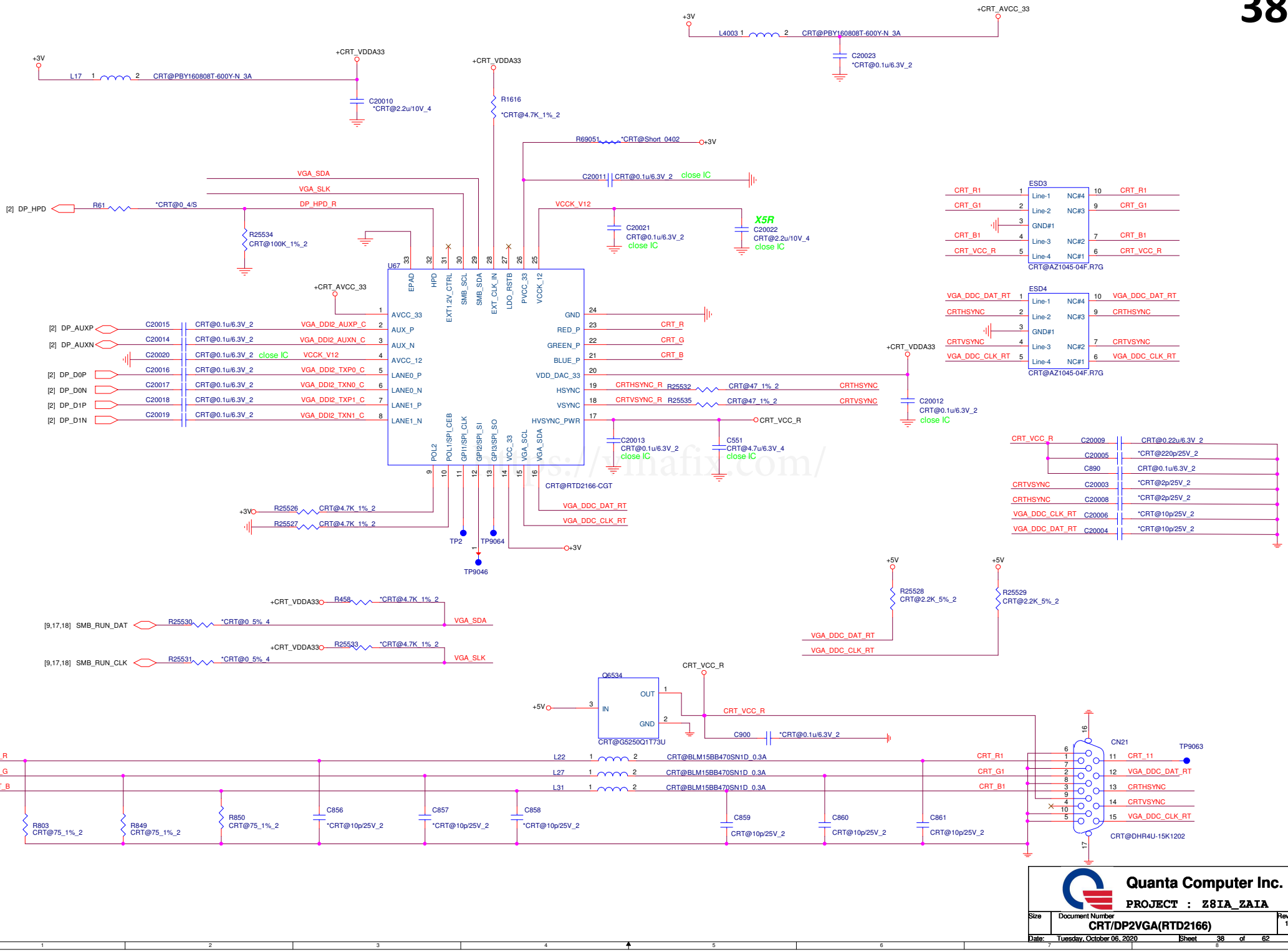
DP TO VGA (CRT)



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Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number: CRT/DP2VGA(RTD2166)	Rev: 1A
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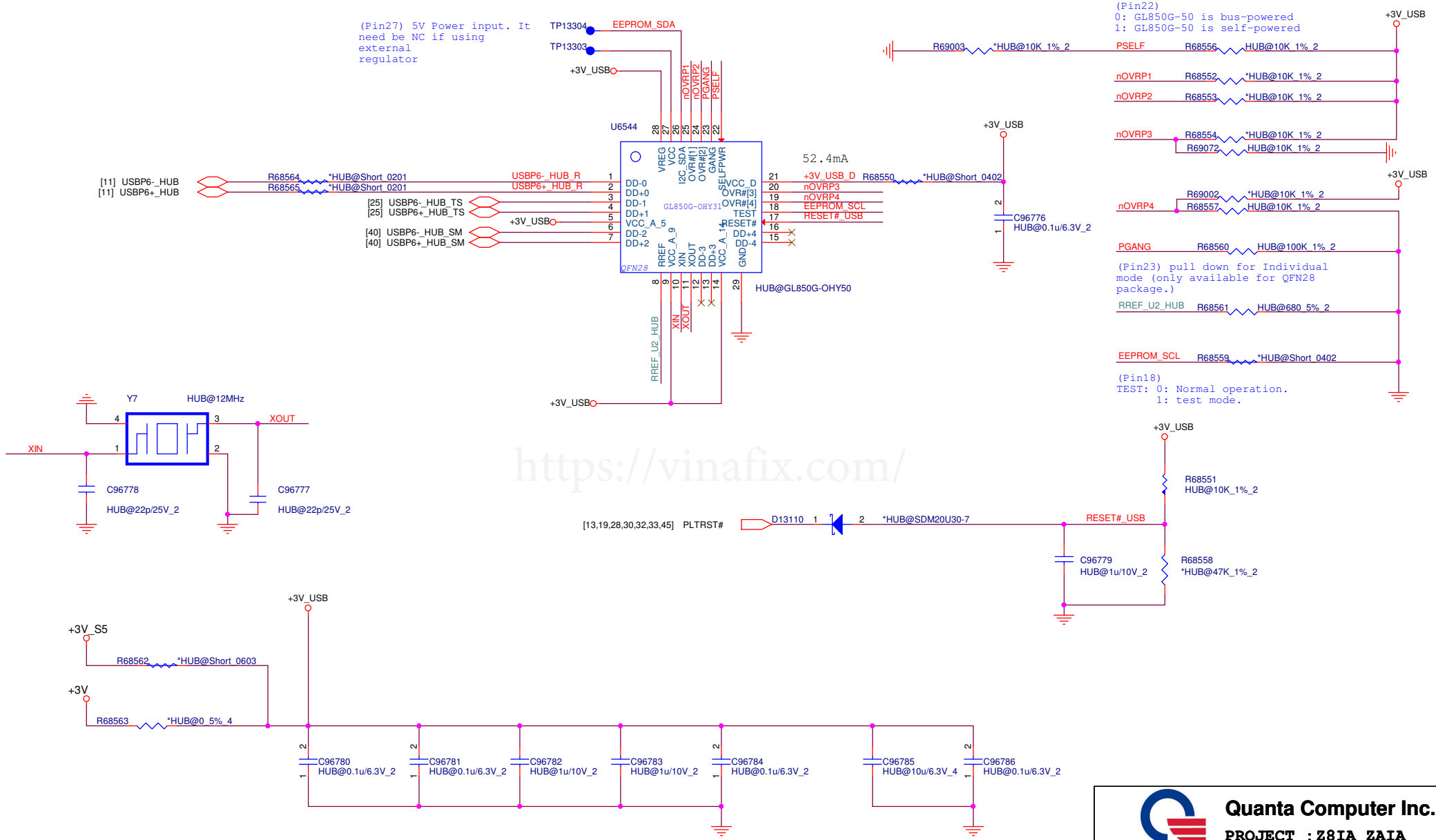
USB HUB



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Quanta Computer Inc.

PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	USB HUB GL850G	1A
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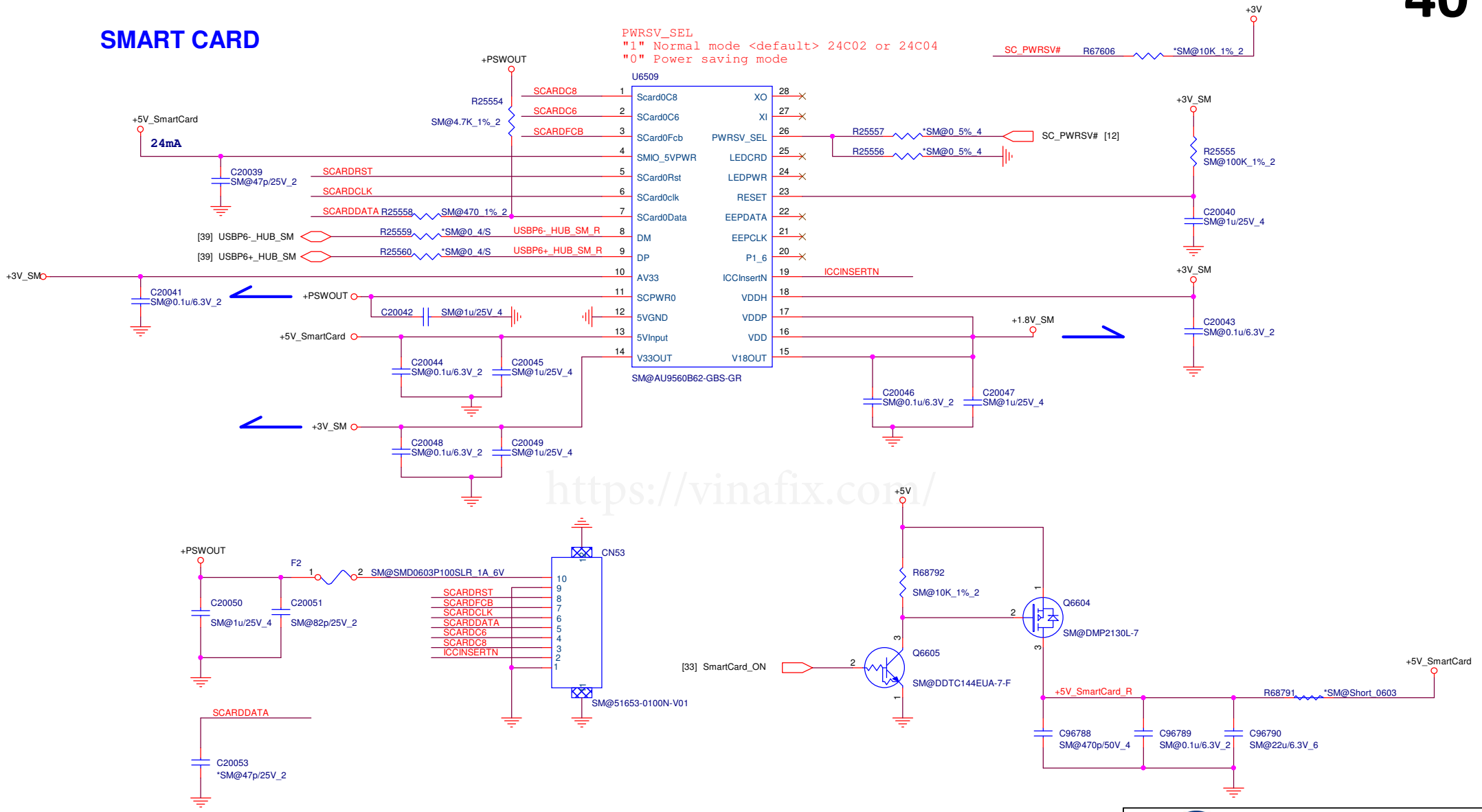
SMART CARD



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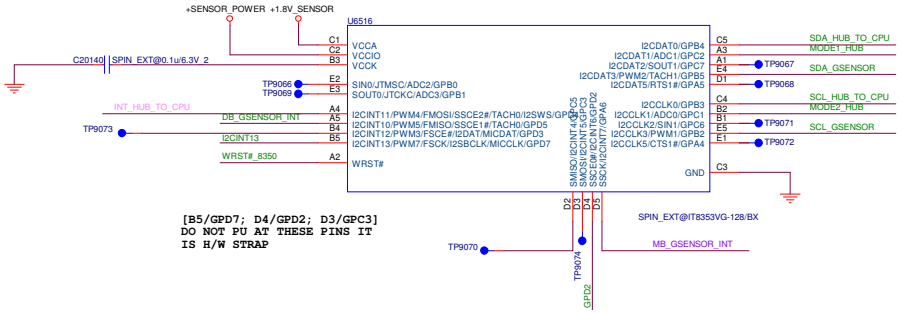
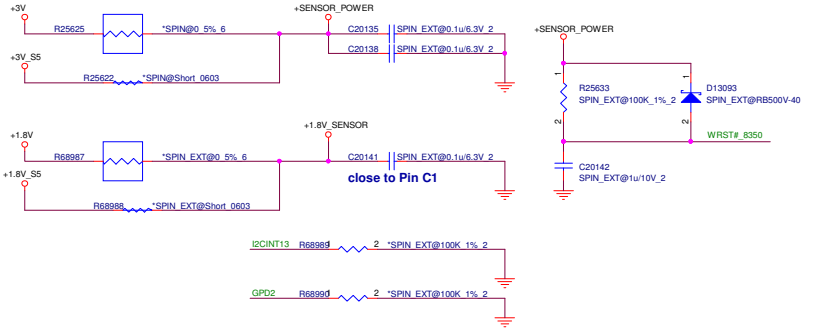
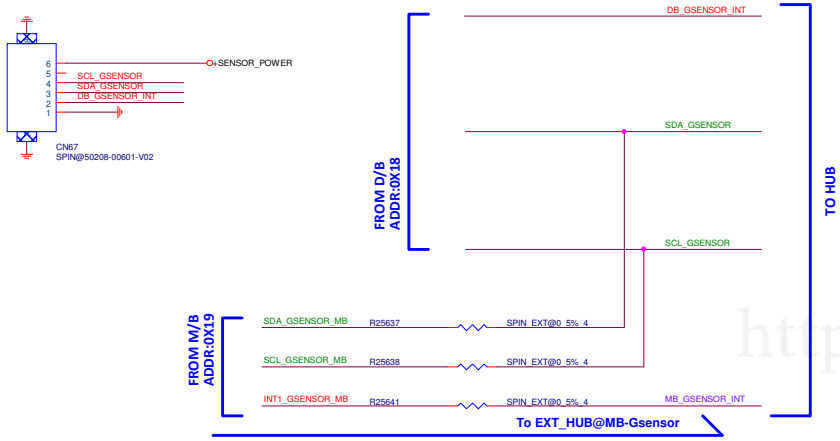
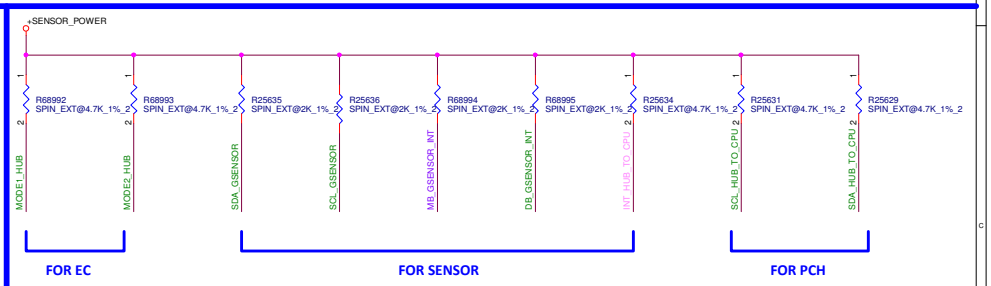
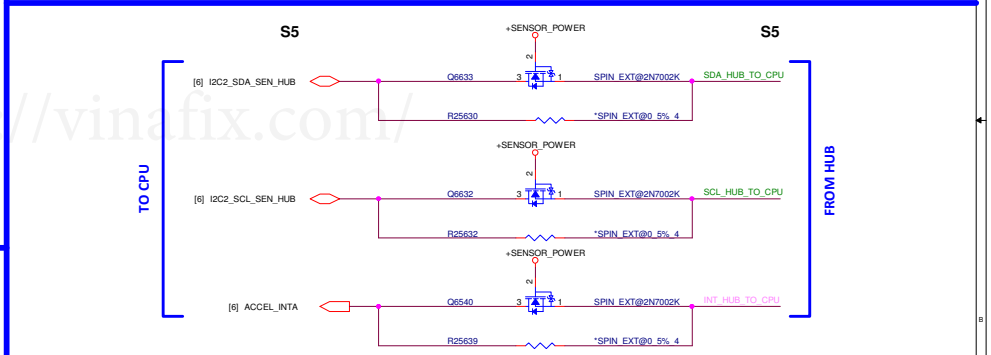
Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number: SMART CARD	Rev: 1A
Date: Tuesday, October 06, 2020	Sheet 40 of 62	

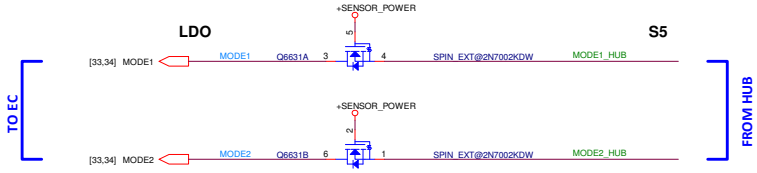


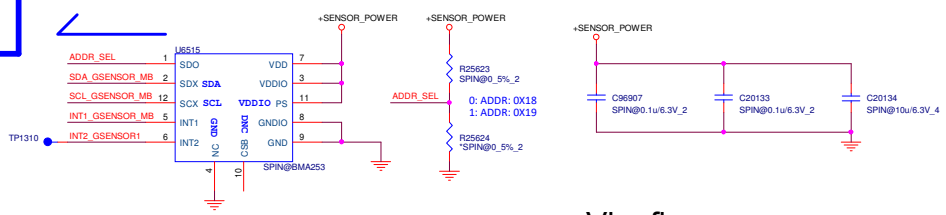




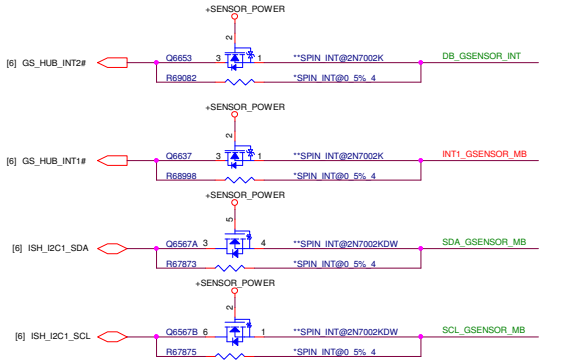


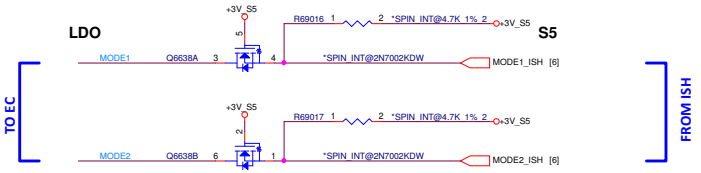






Internal Sensor HUB(Reserve)





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Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number: SENSOR HUB/G Sensor	Rev: 1A
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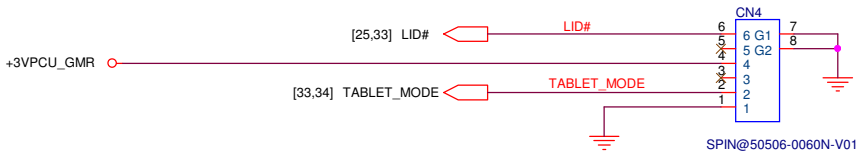
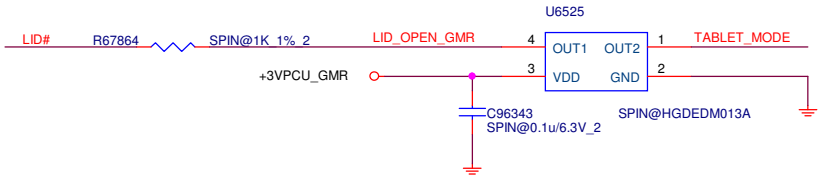
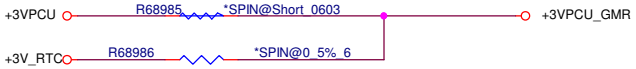
To GMR Board

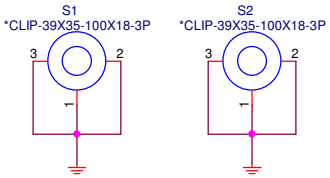


GMR on MB

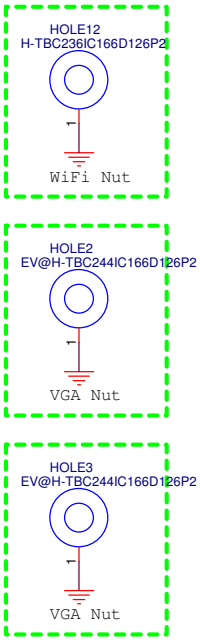


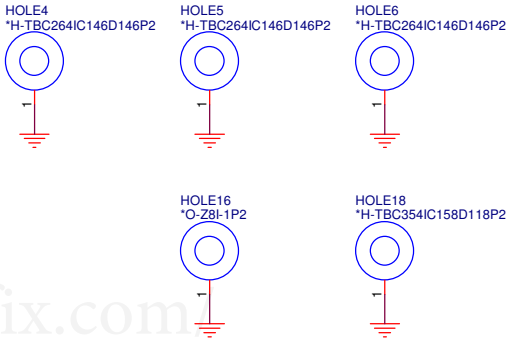


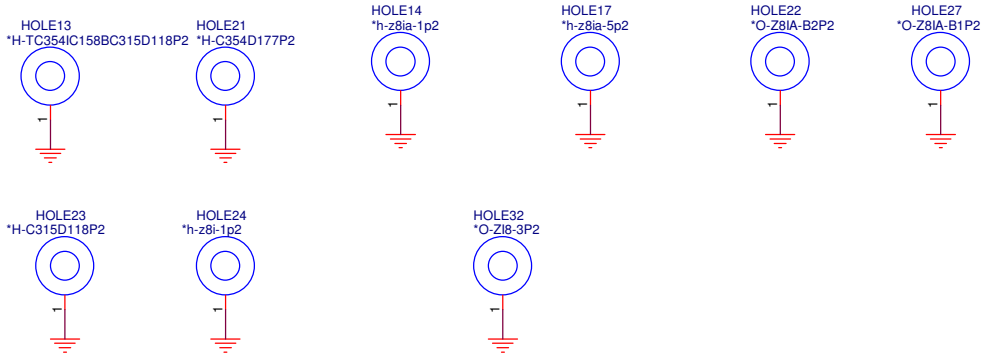
EMI click

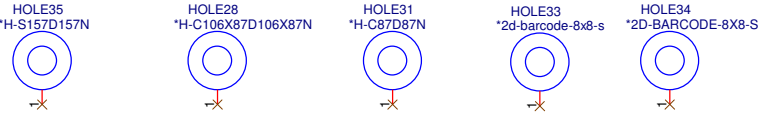


Hole









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Quanta Computer Inc.
PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	GMR Sensor Conn 15	1A
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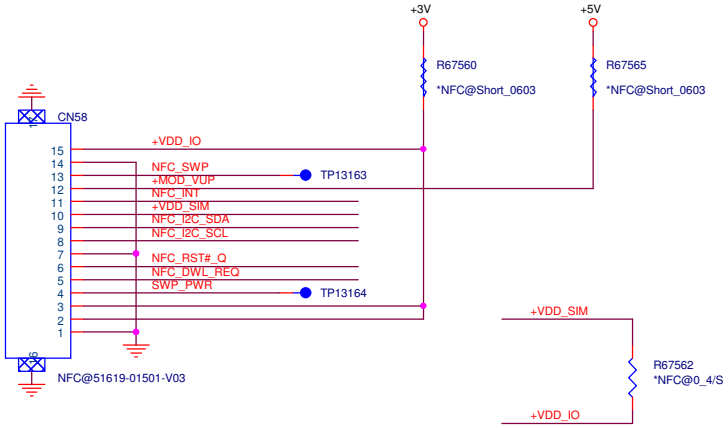
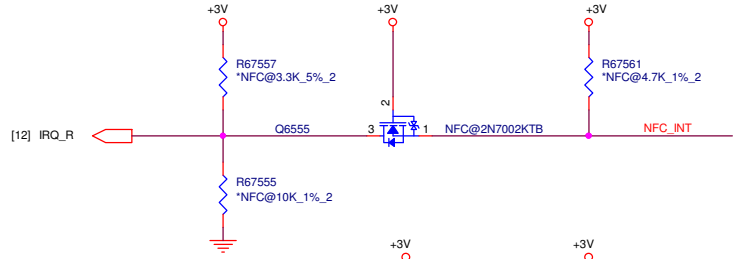
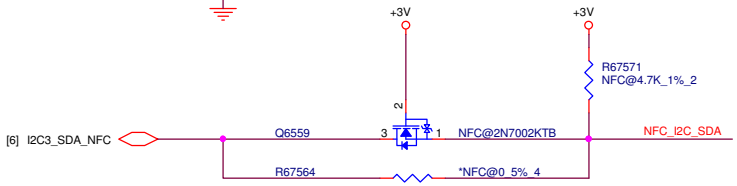
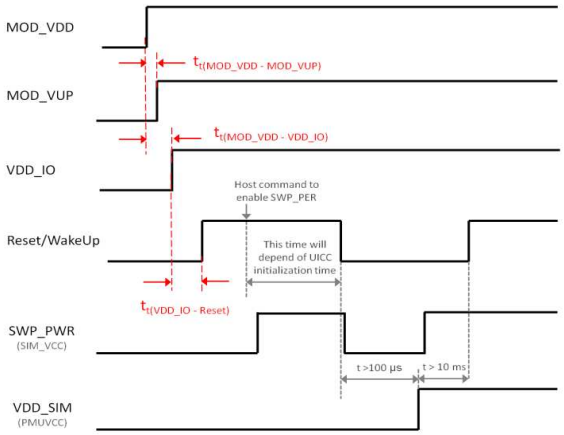


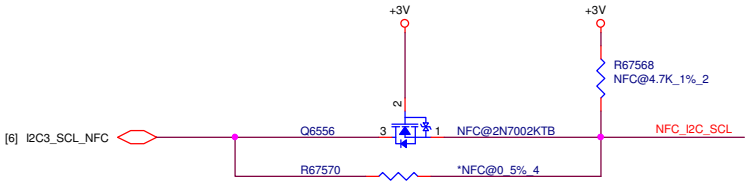




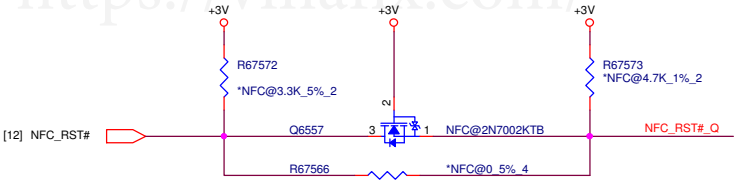
8.1 Power up

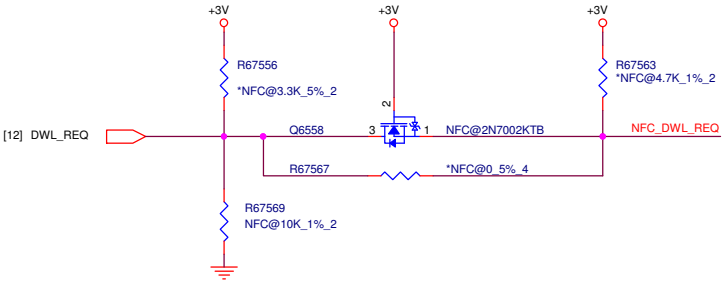


Symbol	Parameter	Min	Typical	Max	Unit
$t_{t(MOD_VDD - MOD_VUP)}$	Minimum time from VDD_MOD high to MOD_VUP high	0	0.5		ms
$t_{t(MOD_VDD - VDD_IO)}$	Minimum time from VDD_MOD high to VDD_IO high	0	0.5		ms
$t_{t(VDD_IO - Reset)}$	Minimum time from VDD_IO high to Reset high	0	0.5		ms

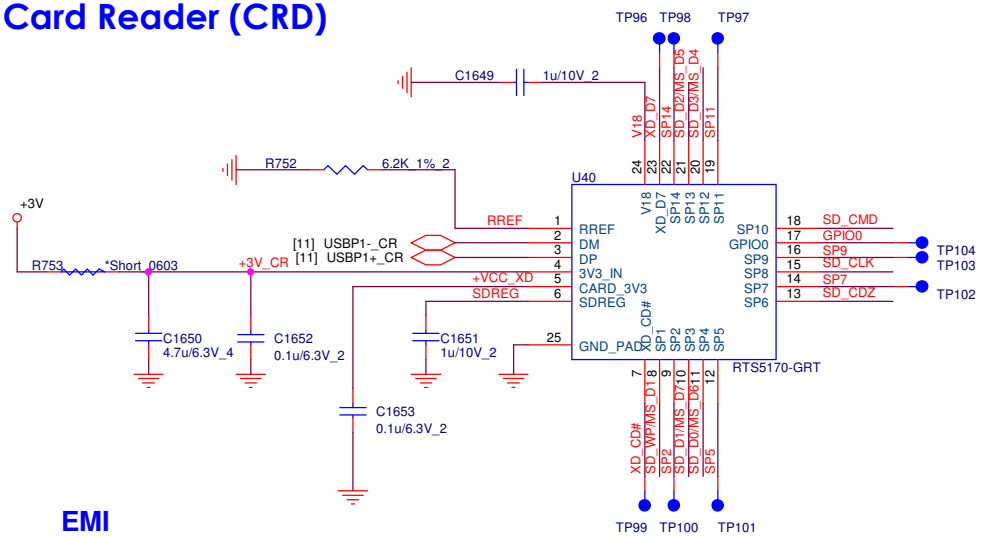


https://vinafix.com/

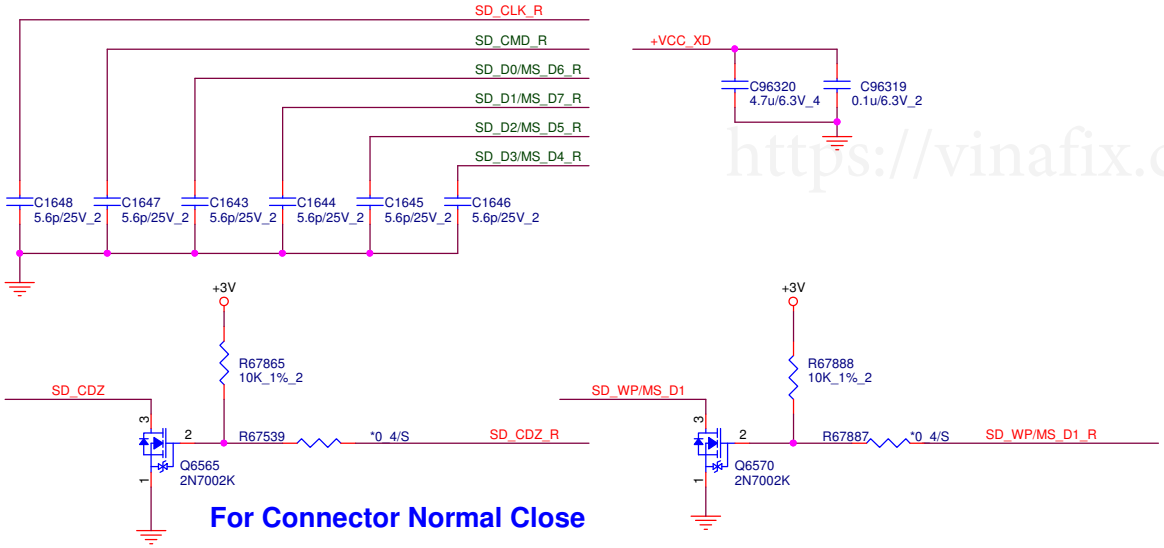




Card Reader (CRD)

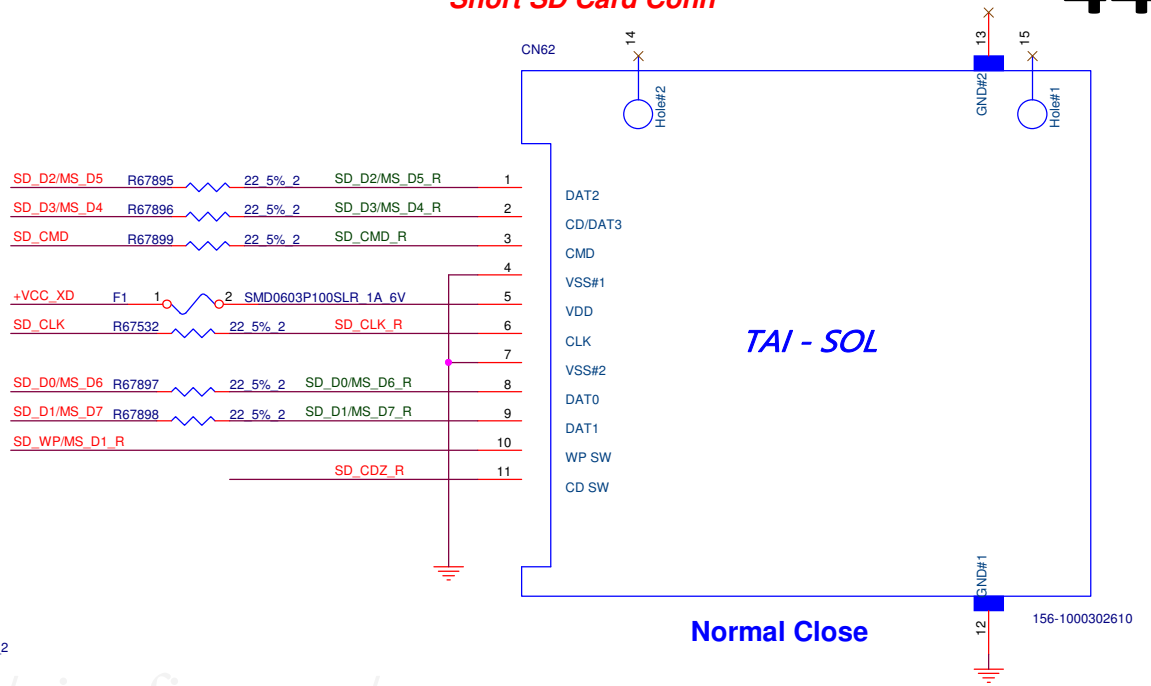


EMI



For Connector Normal Close

Short SD Card Conn



Normal Close

	PROTECT CONTACT		DETECT CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	CLOSE	CLOSE	CLOSE
CARD HALF INSERTION	OPEN	OPEN	CLOSE
CARD INSERTION	CLOSE	OPEN	OPEN

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Quanta Computer Inc.
PROJECT : Z8IA_ZAIA

Size	Document Number	Rev
	CardReader	1A

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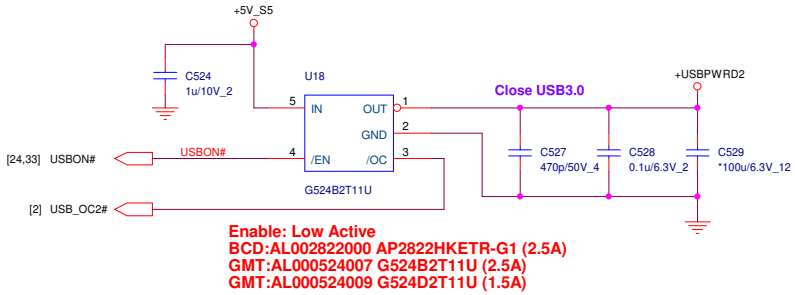
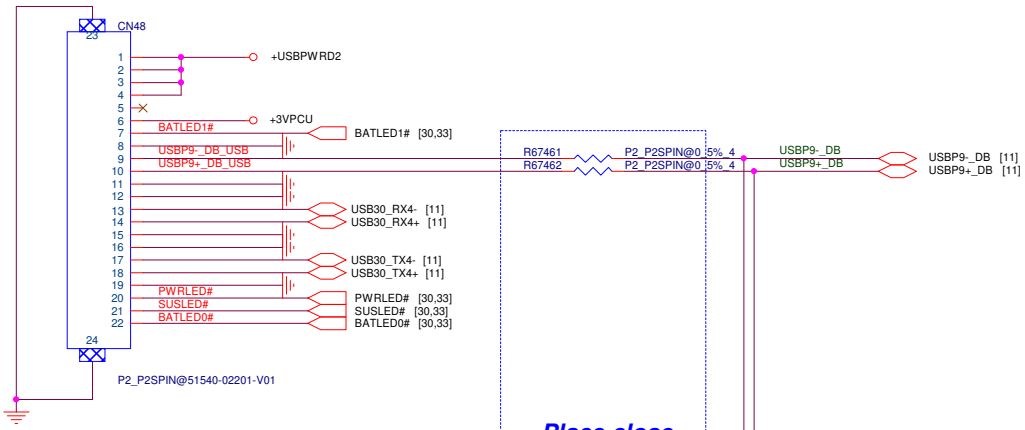
USB3.0 DB (UB3)

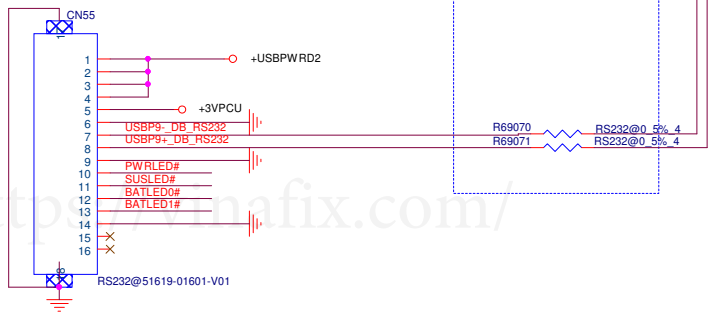


Enable: Low Active
BCD:AL002822000 AP2822HKETR-G1 (2.5A)
GMT:AL000524007 G524B2T11U (2.5A)
GMT:AL000524009 G524D2T11U (1.5A)

USB3.0 DB (UB3)

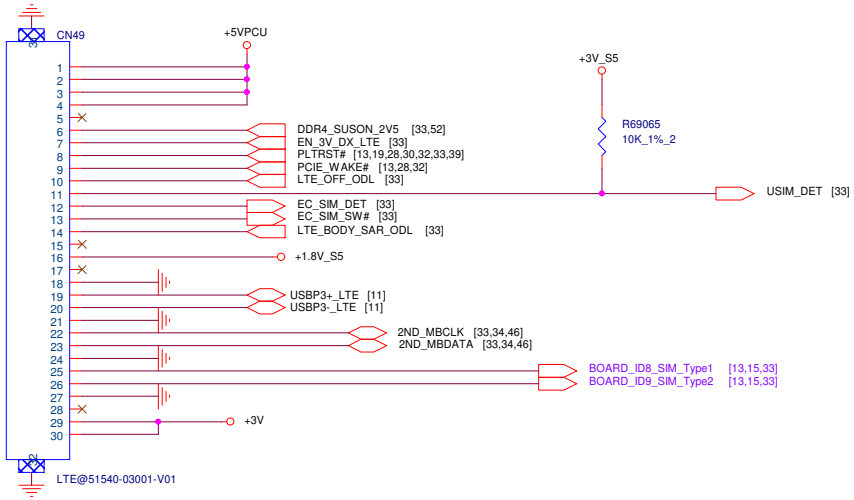


RS232 DB (UB2)



https://vinafix.com/

MB to LTE



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Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number: LTE DB	Rev: 1A
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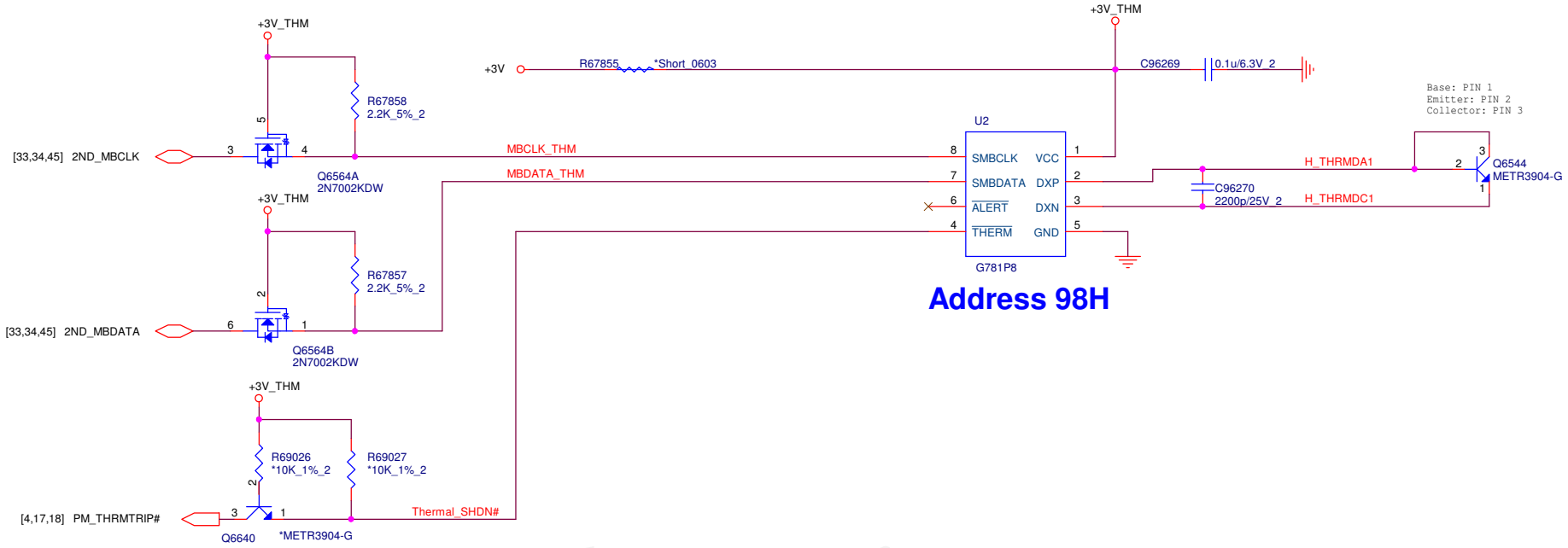
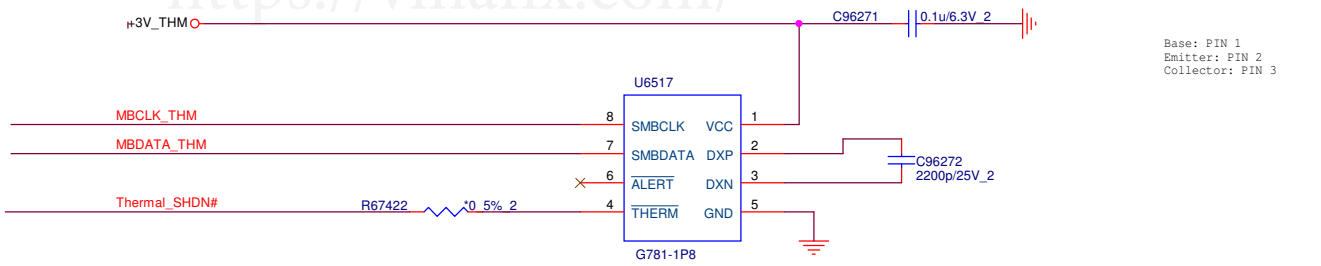
Thermal Sensor(THM)



Address 98H



Address 9AH

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Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number: Thermal Sensor(THM)	Rev: 1A
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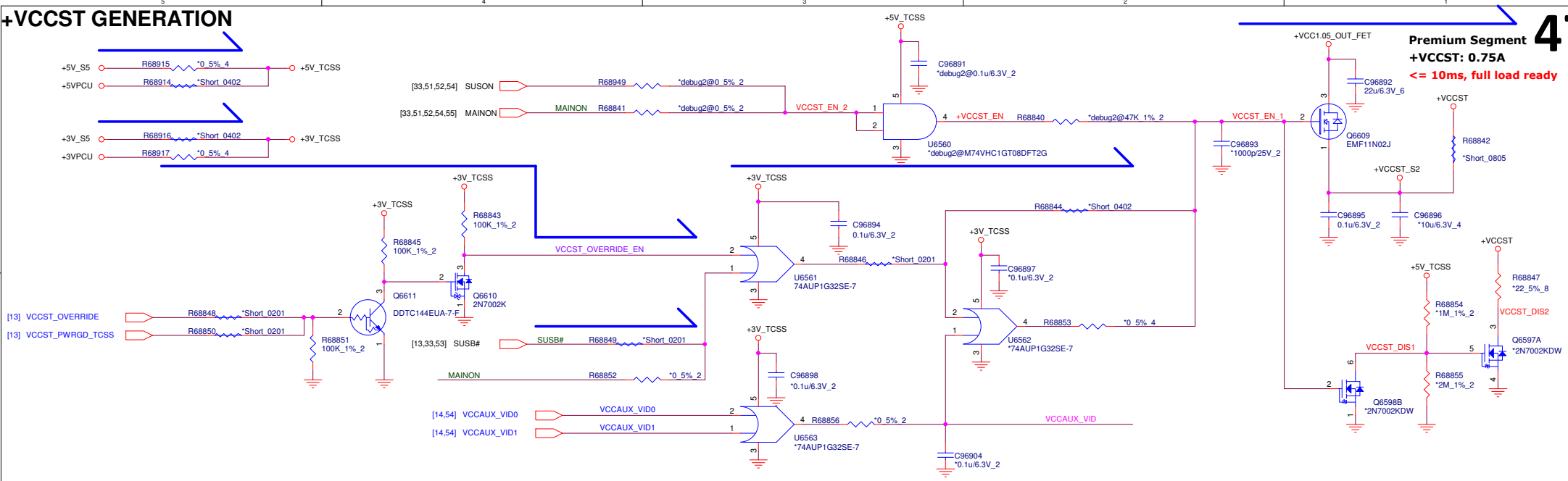
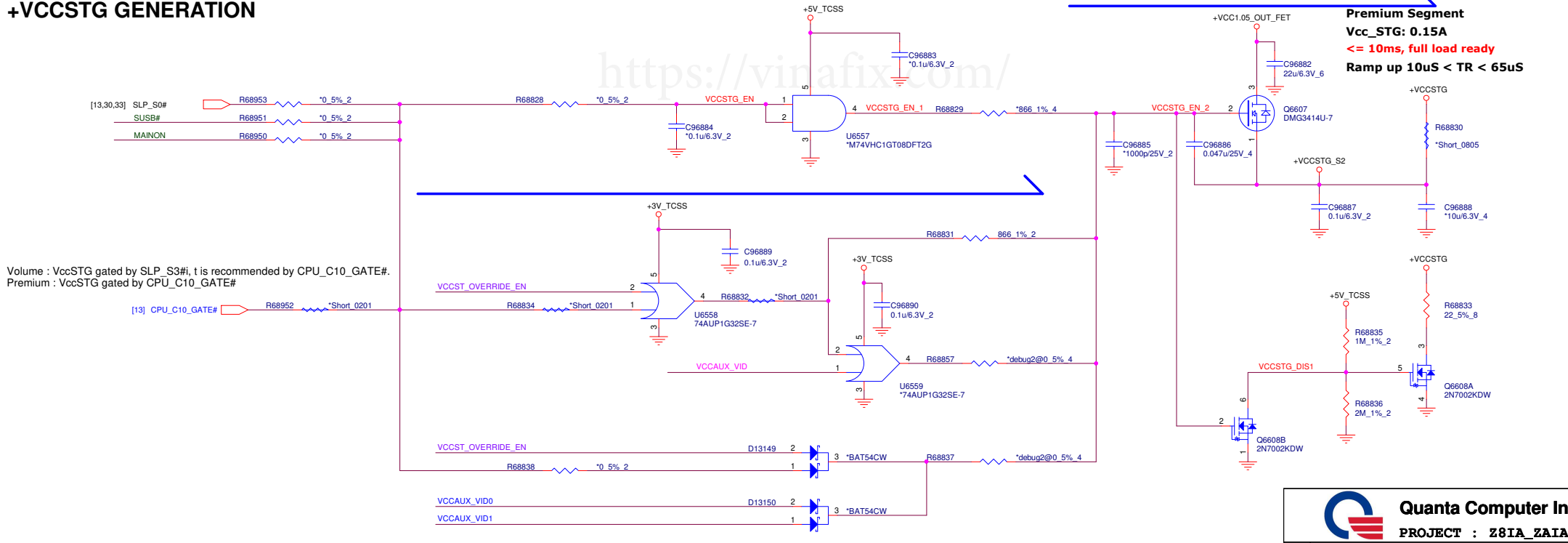
+VCCST GENERATION



Premium Segment
+VCCST: 0.75A
<= 10ms, full load ready

47

+VCCSTG GENERATION



Premium Segment
Vcc_STG: 0.15A
<= 10ms, full load ready
Ramp up 10uS < TR < 65uS

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Quanta Computer Inc.		
PROJECT : Z8IA_ZAIA		
Size	Document Number: VCCST,VCCSTG	Rev: 1A
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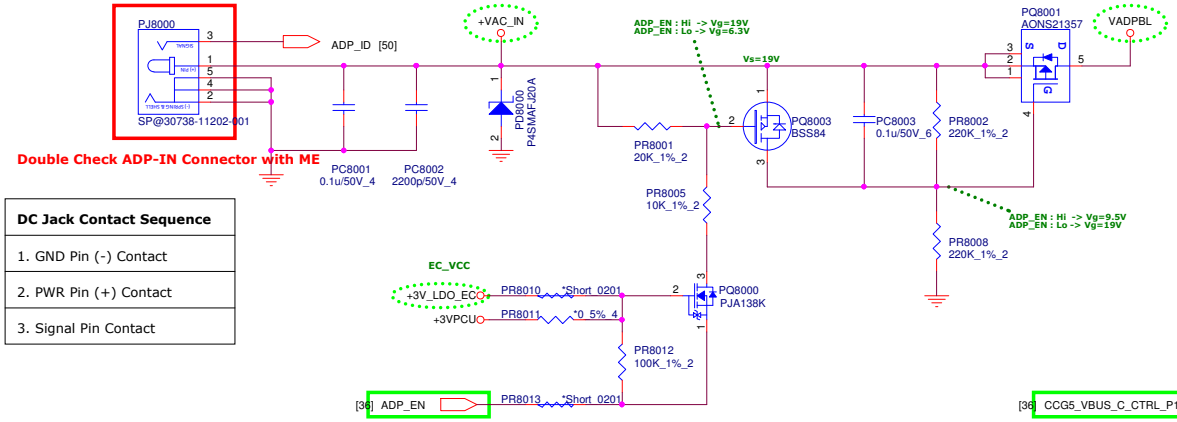
ADP=19V

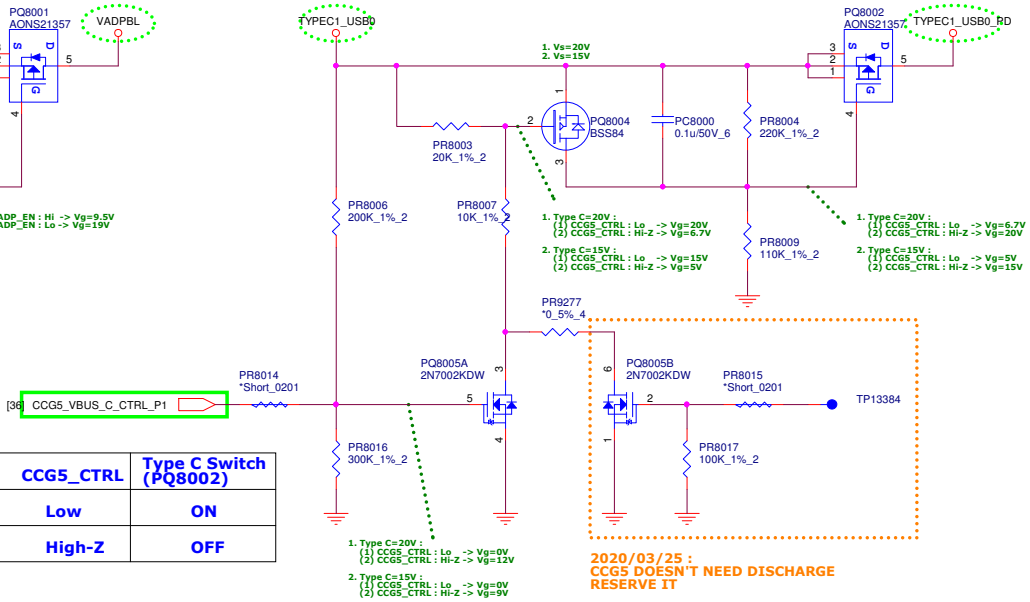


Double Check ADP-IN Connector with ME

DC Jack Contact Sequence
1. GND Pin (-) Contact
2. PWR Pin (+) Contact
3. Signal Pin Contact

ADP_EN	ADP Switch (PQ8001)
Hi	ON
Low	OFF

Type C PD=20V/15V



2020/03/25 :
CCG5 DOESN'T NEED DISCHARGE
RESERVE IT

CCG5_CTRL	Type C Switch (PQ8002)
Low	ON
High-Z	OFF

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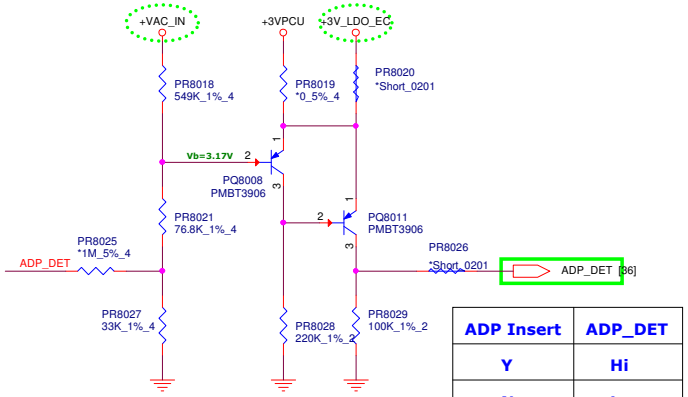
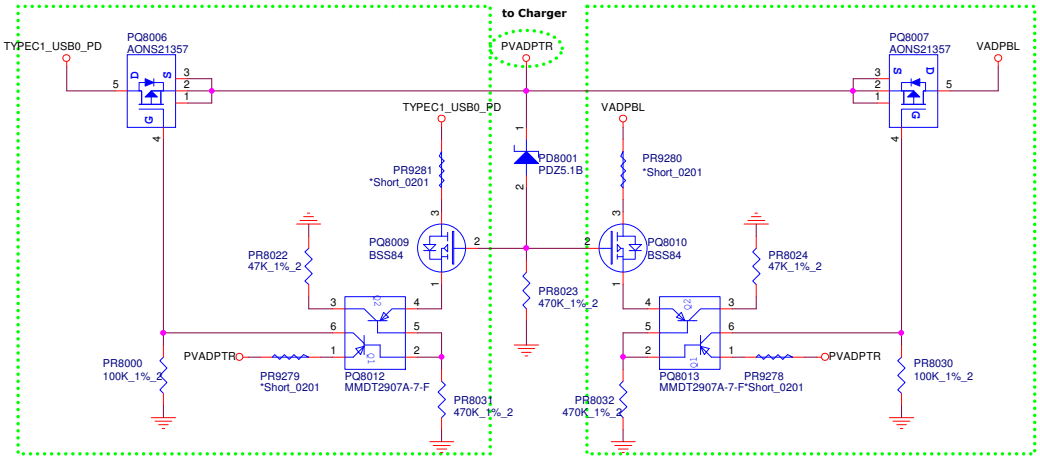


ADP Insert	ADP_DET
Y	Hi
N	Low

Ideal Diode for Type-C Port

Ideal Diode for Adapter



Vi compare	Vo (=PVADPTR)
TYPEC1_USB0 > VADPBL	TYPEC1_USB0
TYPEC1_USB0 < VADPBL	VADPBL

Quanta Computer Inc.
PROJECT : Z8I_ZAI_Z8J

Size	Document Number	Rev
	ADP-IN & TYPE-C	1A
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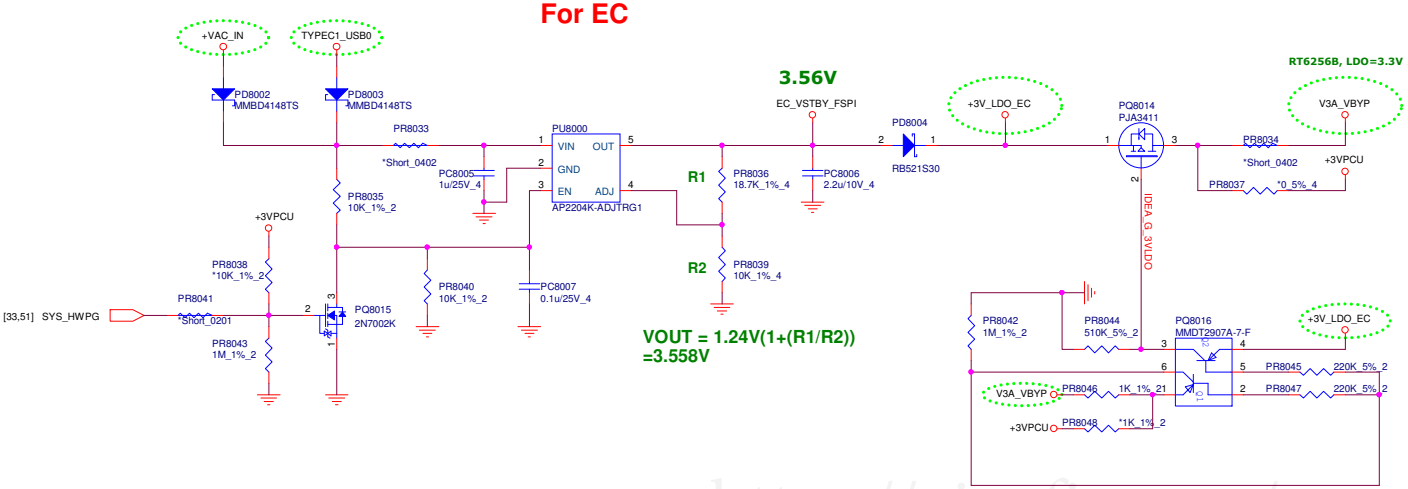
Dead Battery

+VAC_IN [48,50]
TYPEC1_USB0 [36,37,48]
V3A_VBYP [51]
+3V_LDO_EC [33,34,36,48,51]
+3VPCU [12,13,14,25,26,28,30,31,32,33,35,36,37,42,45,47,48,50,51]
+5VPCU [12,24,31,36,37,45,47,51,58]

For EC



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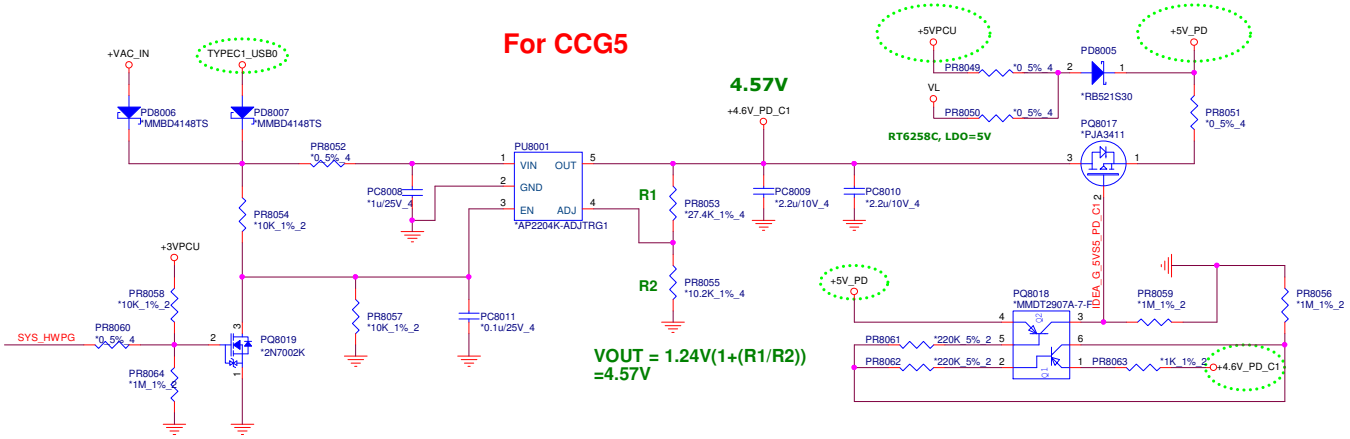
For CCG5



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	Dead Battery	1A
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PR23	UMA	DIS
	20.5K Ohm CS32052FB21	16.9K Ohm CS31692FB11
	78W	95W

(1) BQ24780S : 1 µA/W (default)
(2) RT3612EB : PSYS = 1.6V

CS32052FB21 RES CHIP 20.5K 1/16W +-1%(0402) For 78W
CS31692FB11 RES CHIP 16.9K 1/16W +-1% (0402) For 95W
CS31372FB11 RES CHIP 13.7K 1/16W +-1%(0402) For 116W

ACDET=10.5V

Double Check if BI pin PU Low

Double Check BATT Connector with ME

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

ILIM=0.793V
Rsr = 0.01ohm

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Quanta Computer Inc.			
PROJECT : Z8I_ZAI_Z8J			
Size	Document Number: Charger (BQ24780S)		Rev 1A
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+VIN [25,50,52,53,54,55,56,57,58]
+3VPCU [12,13,14,25,26,28,30,31,32,33,35,36,37,42,45,47,48,49,50]
+5VPCU [12,24,31,36,37,45,47,49,58]
VL [49,55]

+5V [25,26,27,29,31,33,38,40,43,55]
+5V_S5 [13,24,45,47,52,53,54,56,57,58]
+3V [3,4,9,10,11,12,13,15,17,18,20,22,25,26,27,28,29,30,31,32,33,35,38,39,40,41,43,44,45,46,52,53,54,55,56,57,58]
+3V_S5 [3,4,6,8,10,13,14,28,29,30,31,32,33,35,39,41,45,47,52,54,55]

+3VPCU
3.3 Volt +/- 5%
TDC : 6A
Width : 240mil
FSW : 500KHZ

To Thermal Protection

High frequency noise eliminate circuit

Power Auto Recovery
(Stuff on dead battery page)

VCC=5V
(DON'T Connect to External Load)

TDC : 4.03A
PEAK : 5.37A
Width : 180mil

TDC : 3.23A
PEAK : 4.31A
Width : 140mil

Soft-Start

+5VPCU
5 Volt +/- 5%
TDC : 8A
Width : 320mil
FSW : 750KHZ

LDO=5V/100mA

VCC=5V
(DON'T Connect to External Load)

TDC : 4.13A
PEAK : 5.5A
Width : 180mil

TDC : 3.53A
PEAK : 4.7A
Width : 160mil

Soft-Start

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Quanta Computer Inc.
PROJECT : Z8I_ZAI_Z8J
Size: Document Number: SYSTEM (RT6256B/RT6258C) Rev: 1A
Date: Tuesday, October 06, 2020 Sheet 51 of 62

+VIN [25,50,51,53,54,55,56,57,58]
+1.2VSUS [3,5,7,17,18,58]
+VDDQ_VTT [17,18]
+VDDQ [17,18]
+5V_S5 [13,24,45,47,51,53,54,56,57,58]
+3V [3,4,9,10,11,12,13,15,17,18,20,22,25,26,27,28,29,30,31,32,33,35,38,39,40,41,43,44,45,46,51,53,54,55,56,57,58]

+3V
PR5001 100K_1%_2
[33] HWPG_VDDR — PR5002 *Short_0201
[33,45] DDR4_SUSON_2V5 — PR5003 *0_5%_2
[33,47,51,54] SUSON — PR5004 *Short_0201
PC5001 *0.1u/50V_4
PR5006 *0_5%_2
[33,47,51,54,55] MAINON
PC5000 *0.1u/50V_4

OCP=11A
PR5005 316K_1%_4
1P35V_TON
PR5007 499K_1%_4
Fsw=500KHz

+VIN
PJ5001 *short3720
+1.2VSUS_VIN
PC5002 0.1u/50V_4
PC5003 10u/25V_6
PC5004 10u/25V_6
PC5005 2200p/50V_4
PC5007 0.1u/50V_4

+1.2VSUS
1.2 Volt +/- 5%
TDC : 6.22A
PEAK : 8.3A
OCP : 11A
Width : 260mil

TDC : 0.45A
PEAK : 0.6A
Width : 20mil

+VDDQ_VTT
PR9288 *Short_0603
PC5006 10u/6.3V_4

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+VDDQ
PR5009 100_5%_2
PC5013 0.1u/50V_4
PC5014 0.047u/25V_4
PC5017 *10u/6.3V_6
+1.2VSUS_TEMP

PU5001 RT8231BGQW
S3 S5 PGOOD CS TON
VTT VTTSNS VTTGND VTTREF VLDOIN
UGATE BOOT PHASE LGATE VDD
GND VID PGND FB VDDQ PAD

1P35V_S3 — PR5013 *0_5%_2 — 1P35V_S5
[3] DDR_VTTT_PG_CTRL — PR5015 0_5%_2 — 1P35V_S3
PR5014 *Short_0201
PR5016 *Short_0201
+5V_S5 — PR5017 *0_5%_2

1P35V_UGATE
1P35V_BOOT — PR5008 2.2_5%_6 — PC5008 0.1u/50V_4
1P35V_PHASE
1P35V_LGATE
1P35V_VDD — PR5011 *Short_0402 — +5V_S5
PC5019 1u/6.3V_2

PQ5001 AONR32320C
PQ5000 AONR36326C

Isat=22A
PL5000 1uH/11A_7x7x3
PR5010 *4.7_5%_6
PC5018 *680p/50V_6
PR5012 *Short_0201

+1.2VSUS_TEMP
PC5009 0.1u/50V_4
PC5015 22u6.3V_8
PC5010 22u6.3V_8
PC5011 22u6.3V_8
PC5012 22u6.3V_8
PC5016 *330u/2V_7343H1.9
PJ5002 *short3720

Rds(on)=15.9m ohm

1P35V_VDDQ
R1
PR5018 8.2K_1%_2
R2
PR5019 10K_1%_2

Vo=0.675*(1+R1/R2)=1.2285V

VID	Ref. Voltage
High	0.675V
Low	0.75V

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=11A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=11-(2.248/2)*15.9mohm
=157.028mV
Rlimit=157.028mV/5uA*10=314.06Kohm

DDR=1.2285V
R1=8.2K/F_4
R2=10K/F_4

2020/03/25 :
for HDMI re-timer IC
+1.2VSUS
[55] MAIND — MAIND
PQ9087 AOSS32334C
+1.2V
+1.2V [27.55]
TDC : 0.22A
PEAK : 0.29A
Width : 20mil

+2.5VSUS Power Rail For DDR4

+3V_S5 [3,4,6,8,10,13,14,28,29,30,31,32,33,35,39,41,45,47,51,54,55]
+2.5V_SUS [17,18]

+2.5V_SUS
2.5Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

+3V_S5
PR5020 *Short_0603
PC5020 10u/6.3V_4
PR5000 100K_1%_2
[33] HWPG_2.5V
PR5021 *Short_0201
PR5023 *0_5%_2
SUSON
PR5024 *Short_0201
PR5025 *Short_0201
DDR4_SOSON_2V5
PC5024 *0.47u/6.3V_4

PU5000 G5719CTB1U
PG VIN LX EN GND VFB
G5719LX2.5UT

PL5001 2.2uH_2.5x2.0x1.2
PJ5000 *Short_0805
+2.5V_SUS
PR5022 *Short_0201
PC5021 10u/6.3V_6
PC5022 *10u/6.3V_6
PC5023 0.1u/50V_4

PR5026 47.5K_1%_2
R1
PR5027 15K_1%_2
R2

Vo=(0.6(R1+R2)/R2)
=2.5V

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Quanta Computer Inc.
PROJECT : ZGI
Size | Document Number: DDR4_+1.2VSUS (RT8231BGQW) | Rev 1A
Date: Tuesday, October 06, 2020 | Sheet 52 of 62

+VIN [25,50,51,52,54,55,56,57,58]
+VCCIN [5]
+VCCST [4,5,13,47,50]
+5V_S5 [13,24,45,47,51,52,54,56,57,58]
+3V [3,4,9,10,11,12,13,15,17,18,20,22,25,26,27,28,29,30,31,32,33,35,38,39,40,41,43,44,45,46,51,52,54,55,56,57,58]

RT3612EBGQW

+VCCIN
TGL-UP3 Line 4+2 SKU(28W) Performance

TDC : 43A
ICCMAX : 65A
LL=2m
VBOOT= 0V

DCR=1.19m-ohm+/-5%
Isat=35A
PL7001 0.24uH/28A_7x7x3
PL7000 0.24uH/28A_7x7x3

Don't Connect Pin2 to Phase

Close to Phase1 Mosfet
For temp level adjust

LL/IMON Compesation

(1) RT3612EB : PSYS = 1.6V
(2) Double Check PMON Setting with charger

Close to Phase1 Inductor

for LL~2m@Imax=65A
for Imax~66A

Recommand output cap:
a. 1pcs 330uF/2.5V_9m_cap
b. 13pcs 22uF/6.3V MLCC includ EE side
c. Reserve 4pcs 22uF/6.3V MLCC

PR7053 setting

CS32052FB21 RES CHIP 20.5K 1/16W +-1%(0402) For 78W
CS31692FB11 RES CHIP 16.9K 1/16W +-1% (0402) For 95W
CS31372FB11 RES CHIP 13.7K 1/16W +-1%(0402) For 116W

PR7053	UMA	DIS
	20.5K Ohm CS32052FB21	16.9K Ohm CS31692FB11
	78W	95W

Quanta Computer Inc.
PROJECT :
Size | Document Number: CPU VR IC (RT3612EBGQW-03) | Rev 3A
Date: Tuesday, October 06, 2020 | Sheet 53 of 62

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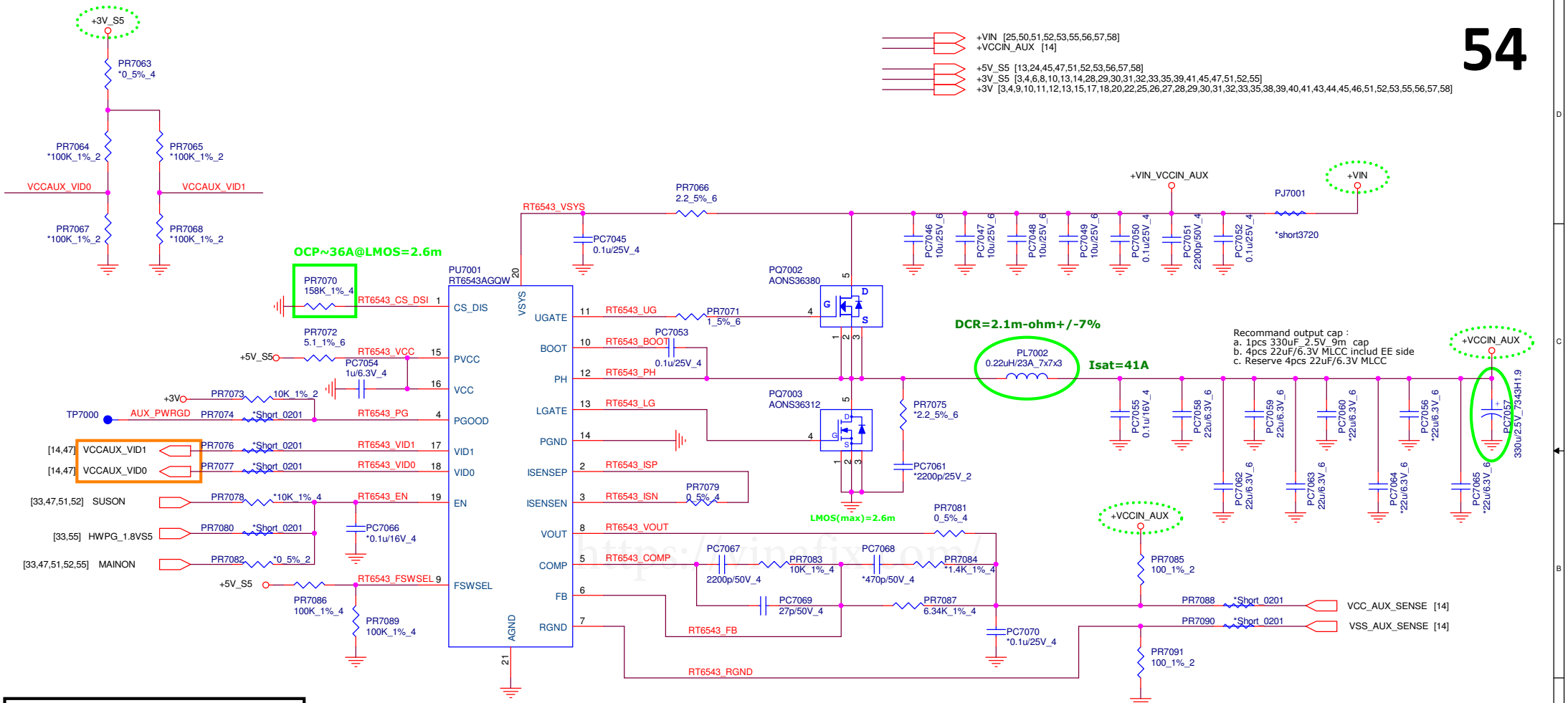
+VIN [25,50,51,52,53,55,56,57,58]
+VCCIN_AUX [14]

+5V_S5 [13,24,45,47,51,52,53,56,57,58]
+3V_S5 [3,4,6,8,10,13,14,28,29,30,31,32,33,35,39,41,45,47,51,52,55]
+3V [3,4,9,10,11,12,13,15,17,18,20,22,25,26,27,28,29,30,31,32,33,35,38,39,40,41,43,44,45,46,51,52,53,55,56,57,58]



+VCCIN_AUX
TGL-UP3 Line 4+2 SKU(28W) Performance

TDC : 16A
ICCMAX : 27A
DC_LL=3.3m
VBOOT=1.8V

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	VCCIN_AUX IC (RT6543AGQW)	3A
Date: Tuesday, October 06, 2020	Sheet 54 of 62	

+3V_S5 [3,4,6,8,10,13,14,28,29,30,31,32,33,35,39,41,45,47,51,52,54]
+1.8V_S5 [14,33,34,41,45,58]
+1.8V [13,22,26,33,41]
+1.5V [26]
+3V [3,4,9,10,11,12,13,15,17,18,20,22,25,26,27,28,29,30,31,32,33,35,38,39,40,41,43,44,45,46,51,52,53,54,56,57,58]
VL [49,51]
+VIN [25,50,51,52,53,54,56,57,58]
+5V [25,26,27,29,31,33,38,40,43,51]

+1.8V_S5
1.8Volt +/- 5%
TDC : 3A
PEAK : 4A
Width : 120mil

Double check PU high with HW

PR9255 100K_1%_2
PR9256 *Short_0201
[33,54] HWPG_1.8VS5
PU3004 JW5213DFND_TRPBF
POK, VIN, SW, NC, FB, PGND, SGND, EPAD, EN
PC551 *2200p/50V_6
PR551 *2.2_5%_6
PL551 1uH/3.35A_2.5x2.0x1.2
5213PG_1.8V
5213LX_1.8V
5213FB_1.8V
5213EN_1.8V
PC272 0.01u/50V_4
PC271 10u/6.3V_4
PC281 0.1u/6.3V_2
PJ9005 *short3720
PR589 *Short_0201
PC574 *22p/50V_4
R1 PR568 20K_1%_4
R2 PR567 10K_1%_2
PC561 0.1u/6.3V_2
PC562 220u/6.3V_6
PC563 22u/6.3V_6
PC9098 *22u/6.3V_6
Vo=0.6*(R1+R2)/R2
=1.8V

PR566 *Short_0201
PU9005 *M74VHC1GT08DFT2G
S5_ON [33,51]
SLP_SUS#_EC [13,33]

TDC : 0.3A
PEAK : 0.4A
Width : 20mil
MAIND
PQ9 AOSS32334C

+1.5V
1.5Volt +/- 5%
TDC : 0.39A
PEAK : 0.52A
Width : 20mil

Double check PU high with HW
[33] HWPG_1.5V
[33,47,51,52,54] MAINON
PR8416 *100K_1%
PR284 *0_5%_2
PR6417 *0_5%_2
PC6229 *0.47u/6.3V_4
PU3003 *JW5222RSOTB_TRPBF
POK, VIN, SW, EN, GND, FB
G5719LX1.5V
PC242 *4.7u/6.3V_4
PC9097 *22p/50V_4
R1 PR6418 *22.6K_1%_2
R2 PR283 *15K_1%_4
Vo=(0.6(R1+R2)/R2)
=1.504V
PL14 2.2uH/1.67A_2.5x2.0x1.2
PR6414 *Short_0201
PC6230 *10u/6.3V_6
PC6229 *10u/6.3V_6
PC6231 *0.1u/16V_4
PJ3008 *0.001_1%_3720
+1.5V
MAIND [52]

PR3020 150_5%_4
VL
PC6228 0.1u/16V_4
PU3002 TMP708AIDBVR
VCC, OT, SET, GND, HYST
PR3021 25.5K_1%_4
PR3022 *Short_0201
SYS_SHDN# [4,33,51]
Rset(Kohm)=0.0012T*T-0.9308T+96.147
=29.4K ohm
HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

Thermal protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=80C

+VIN
+3V
+5V
+1.2V
+1.8V
PR116 1M_5%_6
PR106 *22_5%_8
PR126 *220_5%_8
PR9286 22_5%_8
PR9227 22_5%_8
PR59 1M_5%_6
MAINON_ON_G
MAINON
PQ16 DDTC144EUA-7-F
PR118 1M_5%_6
PR120 *100K_1%_6
PQ12 *2N7002K
PQ19 *2N7002K
PQ9088 2N7002K
PQ9050 2N7002K
PQ6 2N7002K
PC51 2200p/50V_4
ZAUI:Stuff

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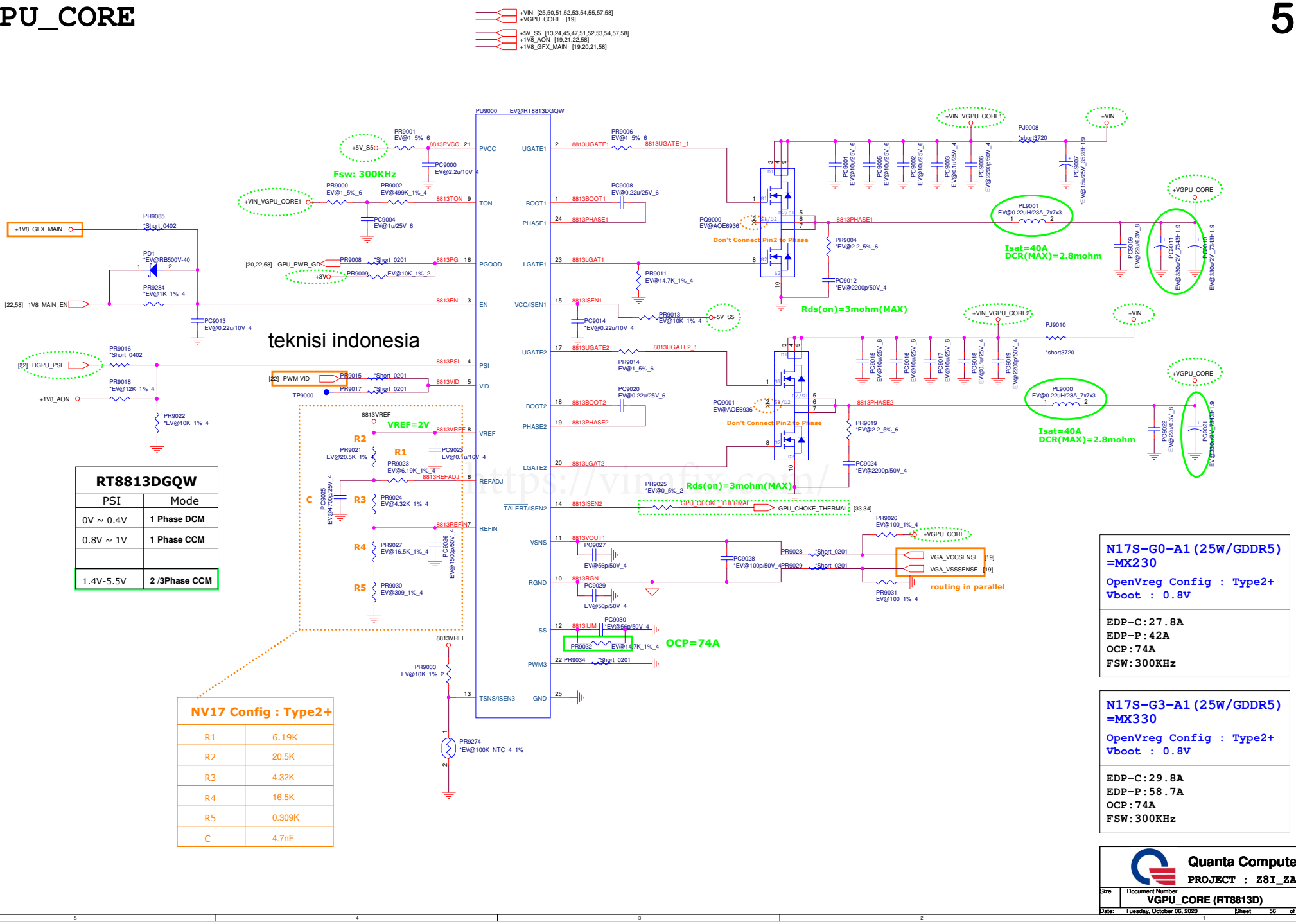
Quanta Computer Inc.
PROJECT : Z8I_ZAI_Z8J
Size | Document Number: +1.8V_S5 /+1.5V/Thermal | Rev 1A
Date: Tuesday, October 06, 2020 | Sheet 55 of 62

VGPU_CORE



RT8813DGQW	
PSI	Mode
0V ~ 0.4V	1 Phase DCM
0.8V ~ 1V	1 Phase CCM
1.4V-5.5V	2 /3Phase CCM

NV17 Config : Type2+	
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	0.309K
C	4.7nF

N17S-G0-A1(25W/GDDR5)
=MX230

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:27.8A
EDP-P:42A
OCP:74A
FSW:300KHz

N17S-G3-A1(25W/GDDR5)
=MX330

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:29.8A
EDP-P:58.7A
OCP:74A
FSW:300KHz

Quanta Computer Inc.
PROJECT : Z8I_ZAI_Z8J

Size	Document Number	Rev
	VGPU_CORE (RT8813D)	1A
Date: Tuesday, October 06, 2020	Sheet 56 of 62	

1.35V_GFX

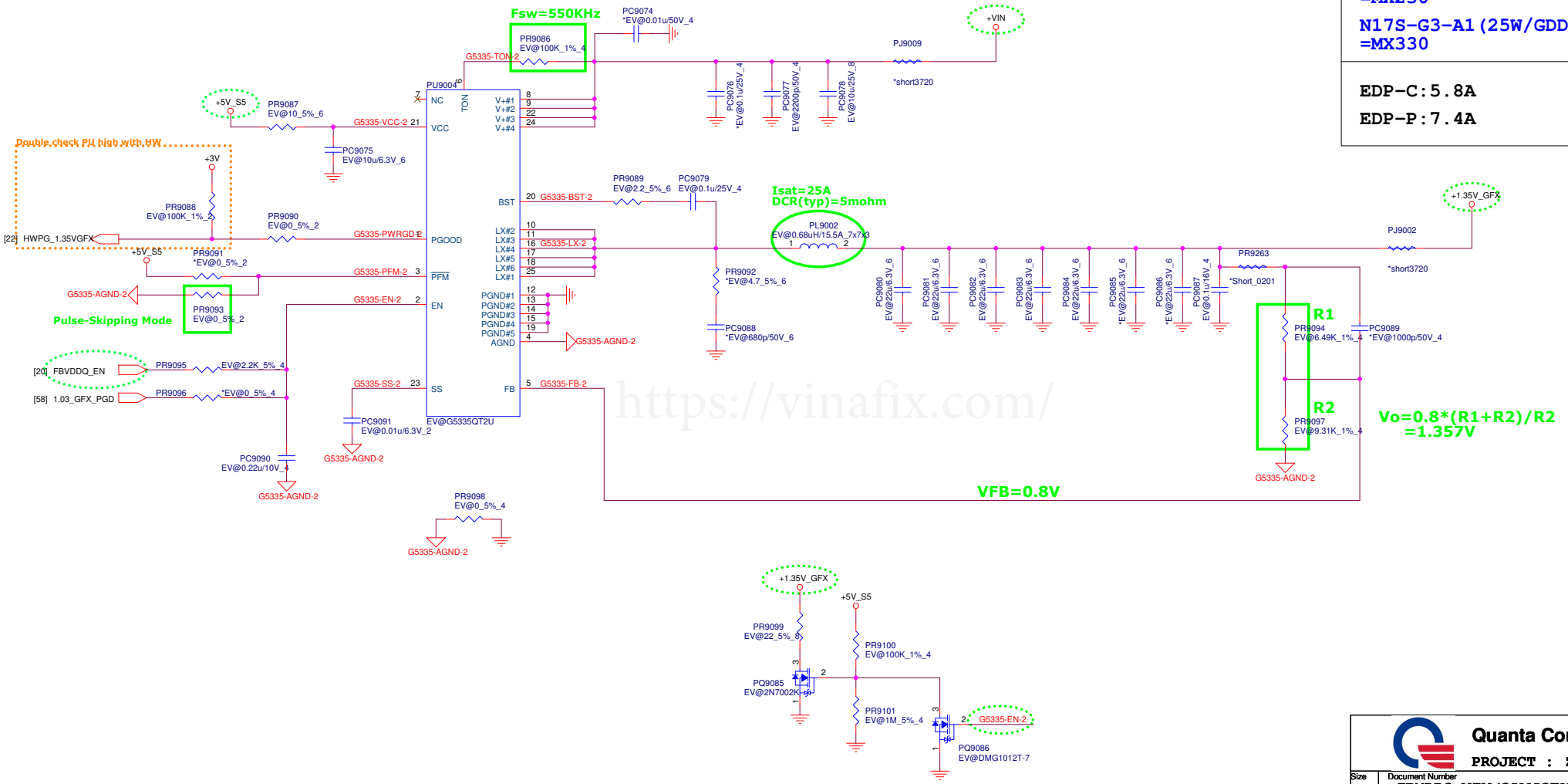
+VIN [25,50,51,52,53,54,55,56,58]
+1.35V_GFX [20,23]
+5V_S5 [13,24,45,47,51,52,53,54,56,58]
+3V [3,4,9,10,11,12,13,15,17,18,20,22,25,26,27,28,29,30,31,32,33,35,38,39,40,41,43,44,45,46,51,52,53,54,55,56,58]

N17S-G0-A1(25W/GDDR5)
=MX230

N17S-G3-A1(25W/GDDR5)
=MX330

EDP-C:5.8A

EDP-P:7.4A



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Quanta Computer Inc.
PROJECT : Z8I_ZAI_Z8J

Size	Document Number	Rev
	FBVDDQ_MEM (G5335QT2U)	1A
Date: Tuesday, October 06, 2020	Sheet 57 of 62	

+1.8V_S5 [14,33,34,41,45,55]
+1V8_GFX_MAIN [19,20,21,56]
+1V8_AON [19,21,22,56]
+5VPCU [12,24,31,36,37,45,47,49,51]
+VIN [25,50,51,52,53,54,55,56,57]

+1.2VSUS [3,5,7,17,18,52]
+1.03_GFX [19]
+5V_S5 [13,24,45,47,51,52,53,54,56,57]
+3V [3,4,9,10,11,12,13,15,17,18,20,22,25,26,27,28,29,30,31,32,33,35,38,39,40,41,43,44,45,46,51,52,53,54,55,56,57]

N17S-G0
N17S-G3

+1.8V_MAIN
TDC : 0.9A
PEAK : 1.2A
Width : 40mil

N17S-G0
N17S-G3

+1.8V_AON
TDC : 0.75A
PEAK : 1A
Width : 40mil

N17S-G0
N17S-G3

+1.03_GFX
TDC : 0.9A
PEAK : 1.1A
Width : 40mil

PU9002
EV@AOZ1331ADI

PU9003
EV@G9336ADJTP1U

PQ9008
EV@AONR32320C

PQ9083
EV@LTC044EUBFS8TL

PQ9084
EV@2N7002KW

PQ9009
EV@2N7002K

PQ9011
EV@2N7002K

PQ9010
EV@DMG1012T-7

PD9001
EV@1SS355

PJ9003
*short3720

Double check PU high with HW

N17S : Vo=(1+R1/R2)*0.5=1.03V

	R1	R2
N17S	133 ohm	124 ohm

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Quanta Computer Inc.
PROJECT : Z8I_ZAI_Z8J

Size	Document Number	Rev
	+1.8V_AON/+1V_GFX	1A

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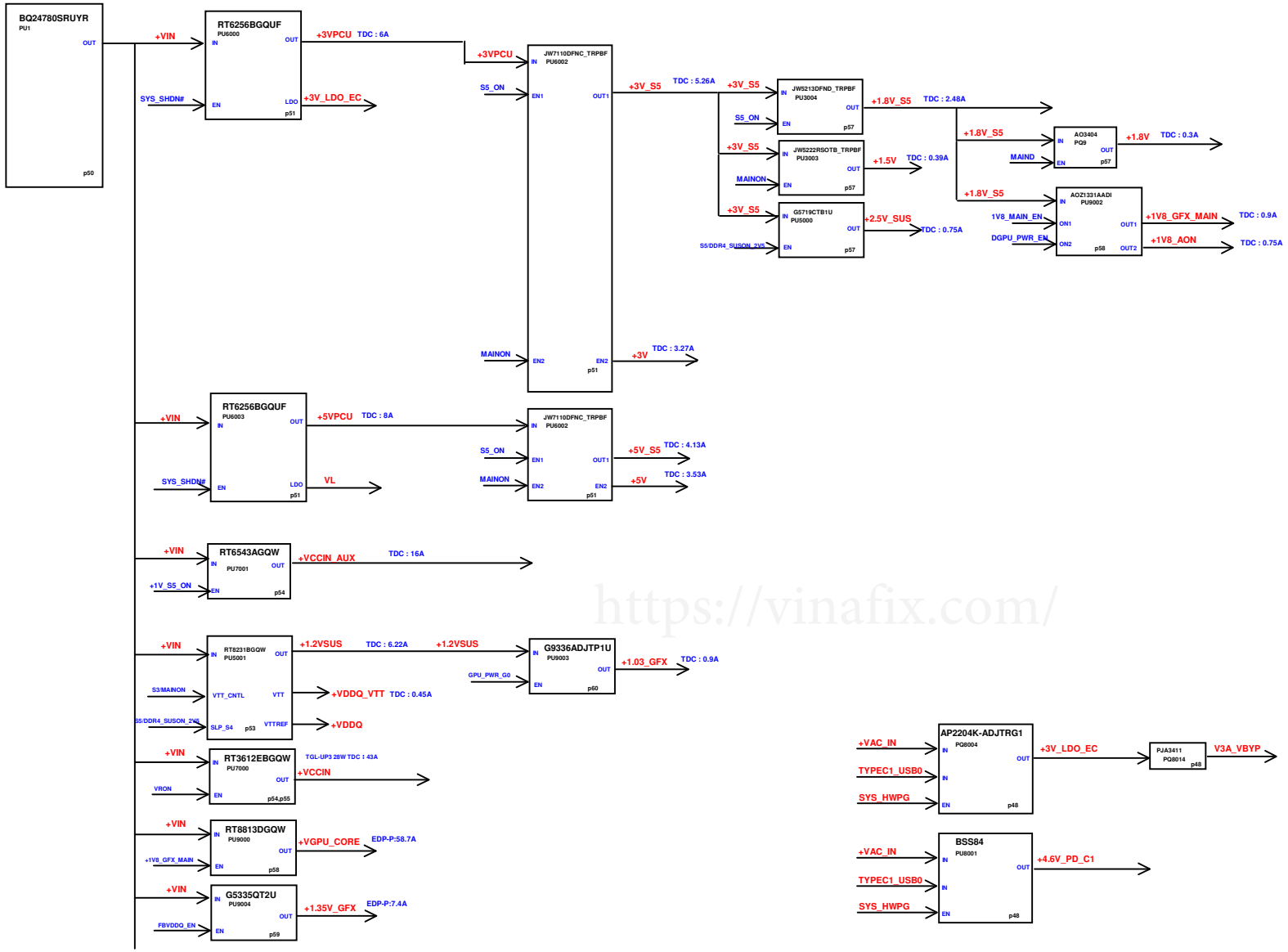

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Quanta Computer Inc.
PROJECT : Z8I_ZAI_Z8J
Size | Document Number | Rev 1A
Power tree
Date: Tuesday, October 06, 2020 | Sheet 59 of 82

Stage	Date	CHANGE LIST
C	7/1	Reserve PCH [TOP_SWAP] pin to EC by Acer request "GPG6"
	7/1	Adjust EC GPIO pin to let Spin function gpio all come out from extension IO IC "GPF2, GPH2, GPJ0, GPD0, GPH0"
	7/1	Change CCG5 power source from [+3V_S5] to [+3V_PCU]
	7/1	Change BBR power enable [CCG5-GPIO P2.3] PU power from [+VCC3V3_SX_TCP0] to [VDD_SUPPLY_1P]
MP	9/22	Change 0 ohm to shortpad

Voltage Rails			
Power Plane	S0	S3	S4/S5
+VIN	N/A	N/A	N/A
BAT-V	N/A	N/A	N/A
+VCC_CORE	ON	OFF	OFF
+VCCGT	ON	OFF	OFF
+VCCSA	ON	OFF	OFF
+SMDDR_VREF_DIMM	ON	OFF	OFF
+1.05V_DEEP_SUS	ON	ON	ON
+1V_SUS	ON	ON	ON
+VCCIO	ON	OFF	OFF
+VCCST	ON	OFF	OFF
+1.2VSUS	ON	ON	OFF
+1.8V_DEEP_SUS	ON	ON	ON
+1.8V_S5	ON	OFF	OFF
+3V_LDO_EC	ON	ON	ON
+3VPCU	ON	ON	ON
+3V	ON	OFF	OFF
+5VPCU	ON	ON	ON
+5V	ON	OFF	OFF
+3V_RTC	ON	ON	ON
+1.03_GFX	ON	OFF	OFF
+1.35V_GFX	ON	OFF	OFF
+1V8_AON	ON	OFF	OFF
+1V8_GFX_MAIN	ON	OFF	OFF
+VGPU_CORE	ON	OFF	OFF

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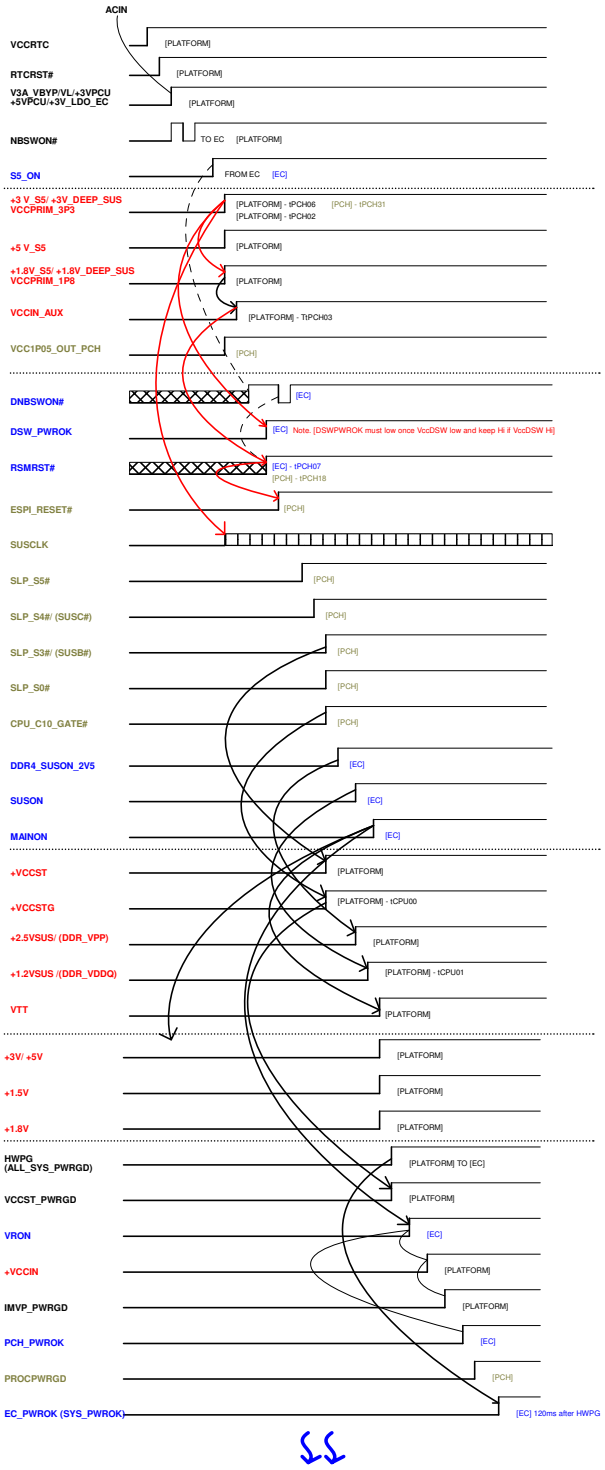

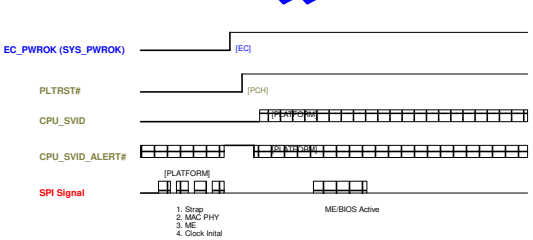

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Quanta Computer Inc.		
PROJECT : ZBIA/ZAIA		
Size	Document Number	Rev
	Power Sequence	1A
Date: Tuesday, October 09, 2018	Sheet 62 of 68	